CB502-NM

Storage Barebone
User's Manual

UM_CB502-NM_v1.1_061126

Document Release History

Release Date	Version	Update Content
February, 2026	1	Released to public.
June, 2026	1.1	Update spec content..

Table of Contents

Preface i
Safety Instructions ii
About This Manual iv
Chapter 1. Product Features 1
1.1 Box Contents 1
1.1.1 Accessory Bag Contents 2
1.2 Specifications 3
1.3 System Block Diagram 4
1.4 Features 5
Chapter 2. Hardware Setup 9
2.1 Central Processing Unit 9
2.2 System Memory 13
2.2.1 Placement 13
2.2.2 DIMM Population 14
2.2.3 Installation 16
2.3 Top Cover 17
2.4 Power Supply Unit 18
2.4.1 Installation 18
2.4.2 LED Indicator 18
2.5 Fan 19
2.6 Disk Drive 20
2.6.1 Disk Drive: 3.5-inch 20
2.6.3 LED Indicator 21
2.6.4 Drive Slot Map 22
2.7 HDD Tray 23
2.8 GPU Card 24
2.9 Slide Rail 25
Chapter 3. Hardware Settings 33
3.1 Block Diagram 33
3.2 Placement 34
3.3 Content List 35
3.4 External Port 37
3.5 Connector Definition 38
3.7 LED 45
3.7.1 Rear Chassis LEDs 45
3.7.2 Internal LEDs 45
3.8 Power board 46
3.8.1 Placement 46
3.8.2 Connector 47
3.9 Fan board 51
3.9.1 Placement 51
3.9.2 Connector 52
3.10 Backplane: 12 Bay 53
3.10.1 Placement 53
3.10.2 Connector 54

3.10.3 LEDs 56
3.10.4 Switchs 57
3.11 IO board 62
3.11.1 Placement 62
3.11.2 Connector 63
3.11.3 LED Button Definition 65
3.11.3 LEDs 66
3.11.4 DIP Switch 67
3.11.5 Fan Mapping 68
Chapter 4. BIOS Configuration Settings 69
4.1 Navigation Keys 69
4.2 BIOS Menu 70
4.2.1 Menu 70
4.2.2 Startup 70
4.3 Main 71
4.3.1 Main 71
4.4 Advanced 72
4.4.1 Trusted Computing 72
4.4.2 PSP Firmware Versions 73
4.4.3 ACPI Settings 73
4.4.4 Redfish Host Interface Settings 73
4.4.5 AMD CBS 74
4.4.6 Serial Port Console Redirection 95
4.4.7 CPU Configuration 95
4.4.8 Debug Port Table Configuration 95
4.4.9 SIO Common Setting 95
4.4.10 SIO Configuration 95
4.4.11 PCI Subsystem Settings 96
4.4.12 USB Configuration 97
4.4.13 Network Stack Configuration 98
4.4.14 NVMe Configuration 98
4.4.15 AMD Mem Configuration Status 98
4.4.16 Tls Auth Configuration 98
4.4.17 RAM Disk Configuration 99
4.4.18 AMD PBS 99
4.4.19 Asmedia 106x Controller #0 100
4.4.20 VLAN Configuration (MAC:020874FB2183) 100
4.4.21 MAC:020874FB2183-IPv4 Network Configuration 100
4.4.22 MAC:020874FB2183-IPv6 Network Configuration 101
4.4.23 Broadcom BCM57416 NetXtreme-E 10GBASE-T RDMA Ethernet Controller-00:15:B2:B4:A4:0A 101
4.4.24 VLAN Configuration (MAC:0015B2B4A40A) 102
4.4.25 MAC:0015B2B4A40A-IPv4 Network Configuration 102
4.4.26 MAC:0015B2B4A40A-IPv6 Network Configuration 103
4.4.27 Broadcom BCM57416 NetXtreme-E 10GBASE-T RDMA Ethernet Controller-00:15:B2:B4:A4:0B 103

4.4.28 VLAN Configuration (MAC:0015B2B4A40B)....104
4.4.29 MAC:0015B2B4A40B-IPv4 Network Configuration....105
4.4.30 MAC:0015B2B4A40B-IPv6 Network Configuration....105
4.4.31 Inter(R) I210 Gigabit Nerwork Connection-00:15:B2:B4:A4:0C....105
4.4.32 VLAN Configuration (MAC:0015B2B4A40C)....105
4.4.33 MAC:0015B2B4A40C-IPv4 Network Configuration....106
4.4.34 MAC:0015B2B4A40C-IPv6 Network Configuration....106
4.4.35 Driver Health....106
4.5 Chipset....107
4.5.1 PCIe Compliance Mode....107
4.5.2 South Bridge....108
4.5.3 North Bridge....109
4.6 Security....110
4.7 Boot....111
4.8 Save & Exit....113
4.9 Server Mgmt....114
4.9.1 BMC Support....114
4.9.2 Wait for BMC....114
4.9.3 FRB-2 Timer....114
4.9.4 OS Watchdog Timer timeout....114
4.9.5 Power Control Policy....115
4.9.6 System Event Log....115
4.9.7 BMC network configurtion....115
4.9.8 View System Event Log....115
4.9.9 BMC Warm Reset....115
4.10 BIOS Post Code....116
Chapter 5. BMC Configuration Settings....148
5.1 Login....148
5.1.1 Required Browser Settings....148
5.1.2 Username and Password....148
5.2 Web UI Common Features....149
5.3 Menu Bar....150
5.4 Dashboard....151
5.5 Sensor....152
5.6 System Inventory....152
5.7 FRU Information....153
5.8 PSU Information....154
5.9 Logs & Reports....155
5.10 Settings....156
5.11 Images Redirection....157
5.12 Chassis Identify....158
5.13 Power Control....159
5.14 Maintenance....160
5.15 Sign Out....161
Chapter 6. Technical Support....162



Copyright © 2026 AIC®, Inc. All Rights Reserved.

This document contains proprietary information about AIC® products and is not to be disclosed or used except in accordance with applicable agreements.

Preface

Copyright

No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electronic, mechanical, photo-static, recording or otherwise, without the prior written consent of the manufacturer.

Trademarks

All products and trade names used in this document are trademarks or registered trademarks of their respective holders.

Changes

The material in this document is for information purposes only and is subject to change without notice.

Warning

1. A shielded-type power cord is required in order to meet FCC emission limits and also to prevent interference to the nearby radio and television reception. It is essential that only the supplied power cord be used.
2. Use only shielded cables to connect I/O devices to this equipment.
3. You are cautioned that changes or modifications not expressly approved by the party responsible for compliance could void your authority to operate the equipment.

Disclaimer

AIC® shall not be liable for technical or editorial errors or omissions contained herein. The information provided is provided "as is" without warranty of any kind. To the extent permitted by law, neither AIC® or its affiliates, subcontractors or suppliers will be liable for incidental, special or consequential damages including downtime cost; lost profits; damages relating to the procurement of substitute products or services; or damages for loss of data, or software restoration. The information in this document is subject to change without notice.

Instruction Symbols

Special attention should be given to the instruction symbols below.

NOTE	This symbol indicates that there is an explanatory or supplementary instruction.
CAUTION	This symbol denotes possible hardware impairment. Upmost precaution must be taken to prevent serious hardware damage.
WARNING	This symbol serves as a warning alert for potential body injury. The user may suffer possible injury from disregard or lack of attention.

Safety Instructions

Before you commence, please attentively read the following important discretions below. All cautions and warnings on the equipment or in the manuals should be circumspectly noted and reviewed.

Always ground yourself to prevent static electricity.
請全程接地，以防止靜電。
请全程接地，以防止静电。
Всегда заземляйте себя, чтобы избежать статического электричества.
Aard jezelf altijd om statische elektriciteit te voorkomen.

- Firmly ground yourself at all times when installing or assembling the internal components of the server. Most of electronic components in the server are highly sensitive to electrical static discharge.
- Use a solid grounding wrist strap and distinctively place all electronic components in static-shielded devices to prevent static. Grounding wrist straps can be purchased in any electronic supply store.
- Confirm that the power source is turned off and then disconnect the power cords from your system before performing any type of installation or manual servicing. A sudden surge of power could severely damage the sensitive electronic components.
- Do not precipitously open the system's top cover. If you must open the cover for maintenance purposes, only a trained technician should be allowed to proceed this action. Integrated circuits on computer boards are highly sensitive to static electricity. Before operating a board or integrated circuit, touch an unpainted portion of the system unit chassis for a couple of seconds to discharge any static electricity on your body.

Place the server in a stable environment.
請將伺服器放置在穩定的環境中。
请将伺服器放置在稳定的环境中。
Поместите сервер в стабильную среду.
Plaats de server in een stabiele omgeving.

- Place this equipment on a stable surface when installing. A small mild drop or fall could cause fatal injury to both the equipment and the person handling the equipment.
- Please keep this equipment away from humidity to prevent vast rust and disintegration.
- Carefully and accurately mount the equipment into the rack. Uneven mechanical loading may lead to hazardous consequences.
- This equipment is to be installed for operation in an environment with maximum ambient temperature below 35°C.
- Review the environment before performing any installation or servicing. Keep the equipment away from hazardous and uneven grounds.
- This server must be installed only in Restricted Access Locations.

Handle equipment with care.
請謹慎操作設備。
请谨慎操作设备。
Обращайтесь с оборудованием осторожно.
Behandel de apparatuur voorzichtig.

- Do not cover the openings of the system. The openings on the system are for air convection, which intentionally protect the equipment from overheating.
- Never pour any liquid into ventilation openings of the system. This could cause catastrophic fire or electrical shock.

- Ensure that the voltage of the power source is within the specification on the label when connecting the equipment to the power outlet. The current load and output power of loads must be within the specification.
- This equipment must be firmly connected to reliable grounding before usage. Pay special attention to power supplied other than direct connections, e.g. using of power strips.
- Place the power cord out of the way of foot traffic. Do not place anything over the power cord. The power cord must be rated for the product, voltage and current marked on the product's electrical ratings label. The voltage and current rating of the cord should be greater than the voltage and current rating marked on the product.

Pay attention to hardware maintenance.
注意硬體維護。
注意硬体维护。
Обратите внимание на обслуживание оборудования.
Besteed aandacht aan hardware-onderhoud.

- If the equipment is not used for a long time, disconnect the equipment from mains to avoid being damaged by transient over-voltage.
- Module and drive bays must not be empty. They must have a dummy cover.
- Never open the equipment without professional assistance. For safety reasons, only qualified service personnel should open the equipment.
- If one of the following situations arise, the equipment should be checked and tested by service personnel:
  1. The power cord or plug is damaged.
  2. Liquid has penetrated the equipment.
  3. The equipment has been exposed to moisture.
  4. The equipment does not work well or will not work according to its user manual.
  5. The equipment has been dropped and/or damaged.
  6. The equipment has obvious signs of breakage.
  7. Please disconnect this equipment from the AC outlet before cleaning. Do not use liquid or detergent for cleaning. The use of a moisture sheet or cloth is recommended for cleaning.

CAUTION
The equipment intended for installation should be placed in Restricted Access Location.

CAUTION
There will be a risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions. After performing any installation or servicing, make sure the enclosure is correct in position before turning on the power.

CAUTION
This unit may have more than one power supply. Disconnect all power sources before maintenance to avoid electric shock.



About This Manual

Thank you for selecting and purchasing the CB502-NM.
This user's manual is provided for professional technicians to perform easy hardware setup, basic system configurations and quick software startup. This document pellucidly presents a brief overview of the product design, device installation and firmware settings for CB502-NM. For the latest version of this user's manual, please refer to the AIC® website: https://www.aicipc.com/en/productdetail/51555.

Chapter 1 Product Features

CB502-NM is a flexible storage server barebone that is specifically designed to accommodate diverse corporations and enterprises for managing heavy workloads and multiple applications.

Chapter 2 Hardware Setup

This chapter displays an easy installation guide for assembling the hardware in this product. Utmost caution for proceeding to set up the hardware is highly advised. Most of the components are highly fragile and vulnerable to exterior influence. Do not endanger the device by placing the device in an unstable environment.

Chapter 3 Motherboard Settings

This chapter elaborates the overall layout of the server motherboard, including multifarious connectors, jumpers and LED descriptions. These descriptions assist users to configure different settings and functions of the motherboard, as well as to confirm the placement of each connector and jumper.

Chapter 4 BIOS Configuration Settings

This chapter introduces the key features of BIOS, including the descriptions and option keys for diverse functions. These details provide users to effortlessly navigate and configure the input/output devices.

Chapter 5 BMC Configuration Settings

This chapter illustrates the diverse functions of IPMI BMC, including the details on logging into the web page and assorted definitions. These descriptions are helpful in configuring various functions through Web GUI without entering the BIOS setup. For more information of BMC configurations, please refer to IPMI BMC (Aspeed AST2500) User's Manual for a more detailed description.

Chapter 6 Technical Support

For more information or suggestion, please contact the nearest AIC® corporation representative in your district or visit the AIC® website: https://www.aicipc.com/en/index.
It is our greatest honor to provide the best service for our customers.

Chapter 1. Product Features

CB502-NM is a high density storage server that includes motherboard, chassis, power supply and disk drive. For more information about our product, please visit our website at https://www.aicipc.com/en/index.

Before removing the subsystem from the shipping carton, visually inspect the physical condition of the shipping carton. Exterior damage to the shipping carton may indicate that the contents of the carton are damaged. If any damage is found, do not remove the components; contact the dealer where the subsystem was purchased for further instructions. Before continuing, first unpack the subsystem and verify that the number of components in the shipping carton is accurate and in good condition.

1.1 Box Contents

This product contains the components listed below.

Please confirm the number and the condition of the components before installation.

	Pre-installed into the system	Number
✓	9600W (3+1 3200W modules) redundant power supply 80+ Titanium	3+1
✓	3.5-inch disk drive tray	12
✓	Heat sink	2
✓	hot swap fans (10 x 80x56mm)	10
✓	AIC® Norma motherboard	1
	Accessory Item	**Number**
✓	EPE foam for front board: 585*440*110H	1
✓	EPE foam for rear board: 585*440*110H	1
✓	EPE foam for front tray: 585*440*200H	1
✓	EPE foam for rear tray: 585*440*200H	1
✓	EPE PAD for rail: 150*135*30T	1
✓	EPE PAD: 130*100*50T	1
✓	37-inch tool-less slide rail assembly	1

1.1.1 Accessory Bag Contents

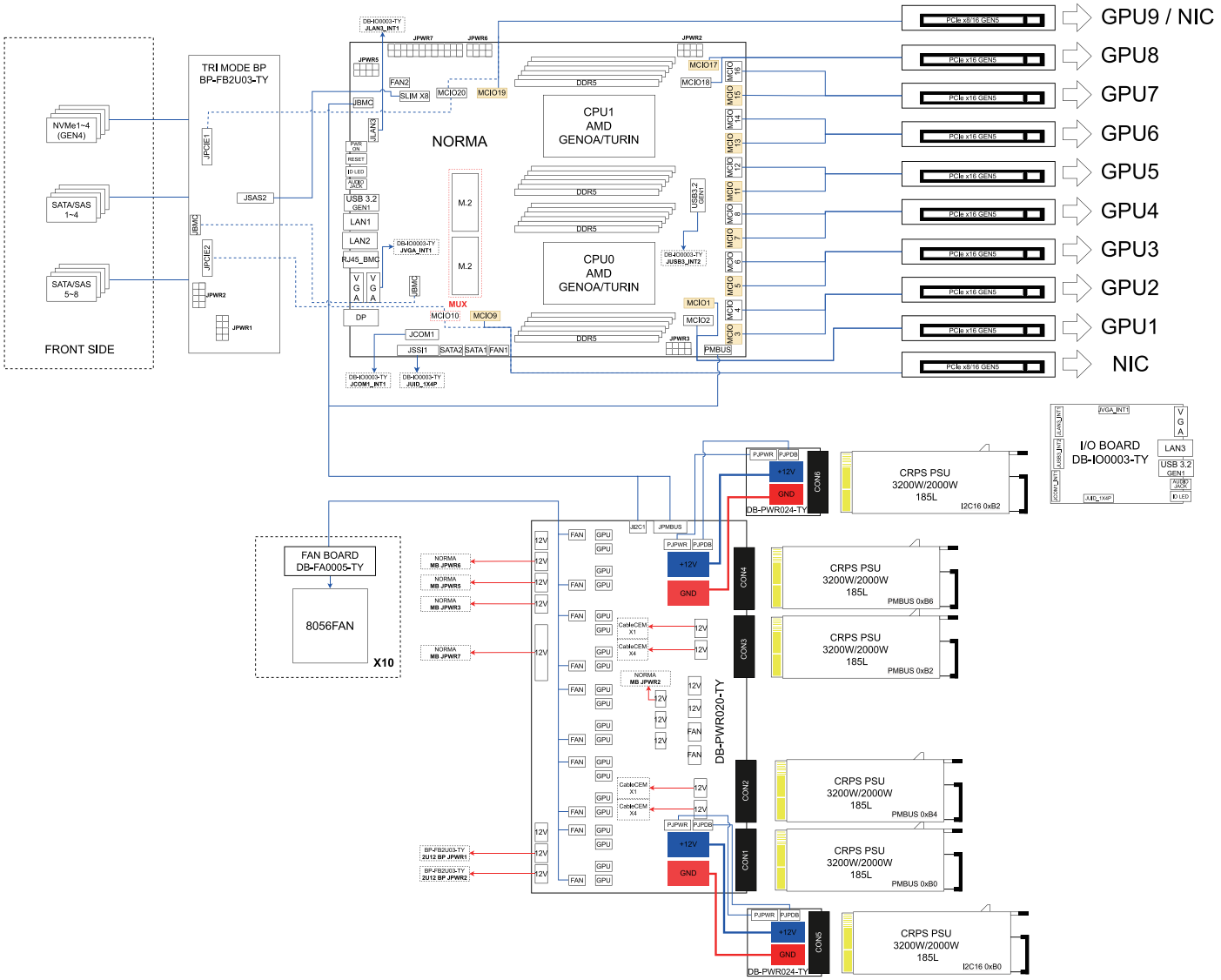
Item	Part No.	Description	Number
ACCESSARY	M15-1698-001X02	ACC	1 set
GPU_BKT_ASSY	M06-1698-008X02	ASS'Y,PART	1 set
GPU_BKT_BACK	H32-1698-010X02	PART	10 pcs
GPU_BKT_BACK	H32-1698-01CX02	RIVETING	10 pcs
SGC 400	H01G61200001	1650X1220/ T=1.2/18.96KG	0.0313 pcs
PILOT PIN/BOT_KNURL	H61K41090R02	Ø4.0*9.0MM	10 pcs
GPU_SINGLE_BKT_BACK	H32-1698-020X01	PART	1 pcs
GPU_SINGLE_BKT_BACK	H32-1698-02CX01	RIVETING	1 pcs
SGC 400	H01G61200001	1650X1220/ T=1.2/18.96KG	0.0060 pcs
PILOT PIN/BOT_KNURL	H61K41090R02	Ø4.0*9.0MM	1 pcs
GPU_SINGLE_BACK_MB	H28-1698-400X01	PART	1 pcs
GPU_SINGLE_BACK_MB	H28-1698-40BX01	BENDING	1 pcs
SGC 400	H01G61000001	1520X1220/ T=1.0/14.56KG	0.0026 pcs
RIVET_DFH/STQ4-5024	H44332024R01	Ø3.2X2.4L/GRIP RANGE:1.6-2.5MM/ SLEEVE:ST	12 pcs
SCREW/MECH	H38W0P304002	RW(+),M3X4L,NI	24 pcs
NYLOK LOCKING SCREW	H39F0PF04004	F(+),632X4L,NI,NYLOK	12 pcs
1 ZIPPER BAG	H81-Z-040001	5(O/W)*7CM,T=0.04MM	2 pcs
5 ZIPPER BAG	H81-Z-040007	10(O/W)*14CM,T=0.04MM	1 pcs
8 ZIPPER BAG	H81-Z-040009	17(O/W)*24CM,T=0.04MM	1 pcs
BUBBLE BAG	H81-B-000005	21(O/W)*25+25CM	1 pcs

Product features are subject to change without notice.

1.2 Specifications

For detailed product specifications and features, please visit the AIC product page:
https://www.aicipc.com/products-detail/cb502-nm/

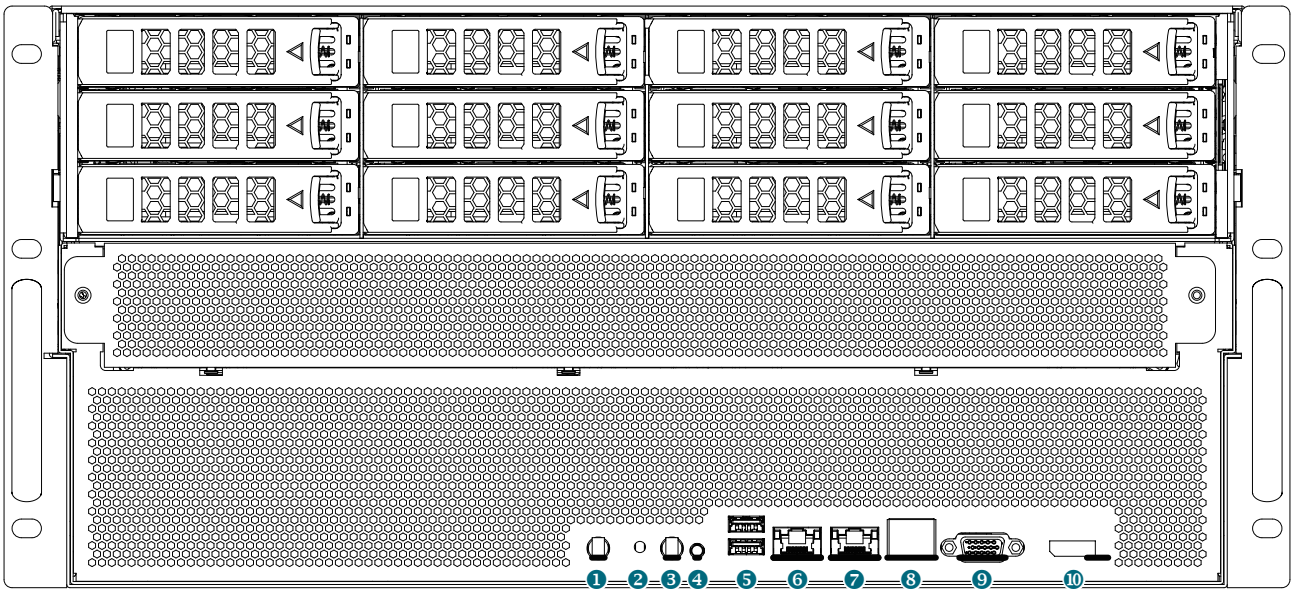
1.3 System Block Diagram



1.4 Features

For detailed product specifications and features, please visit the AIC product page:
https://www.aicipc.com/products-detail/cb502-nm/

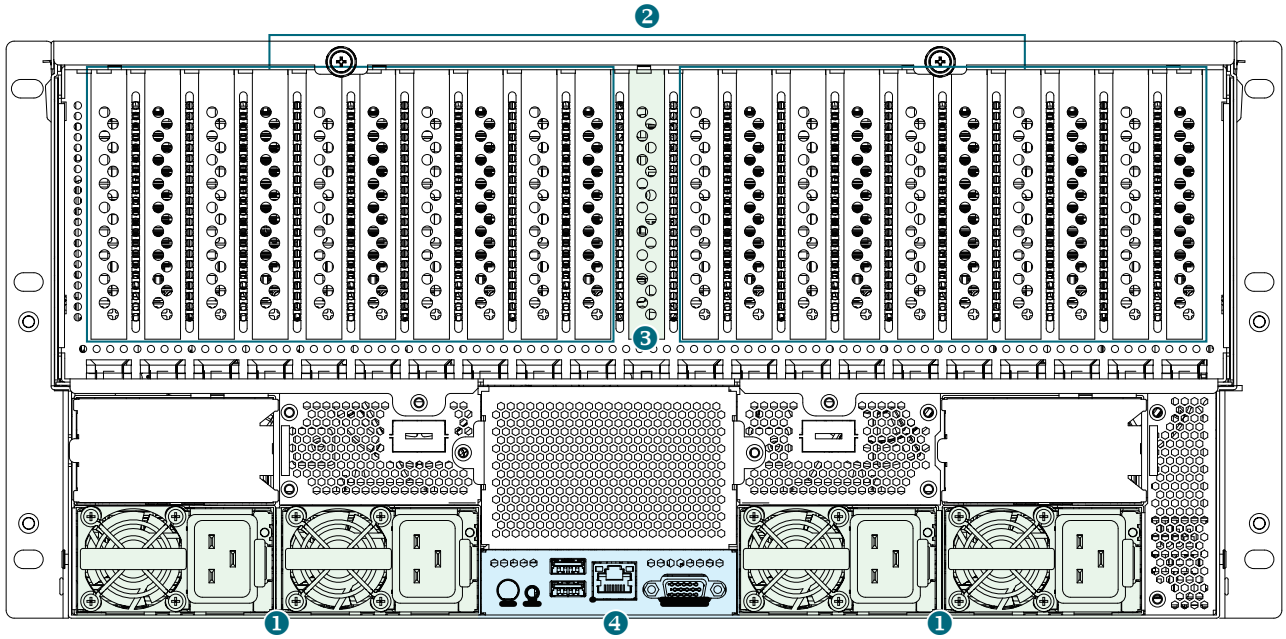
Front Panel



System LED Indicator and switch

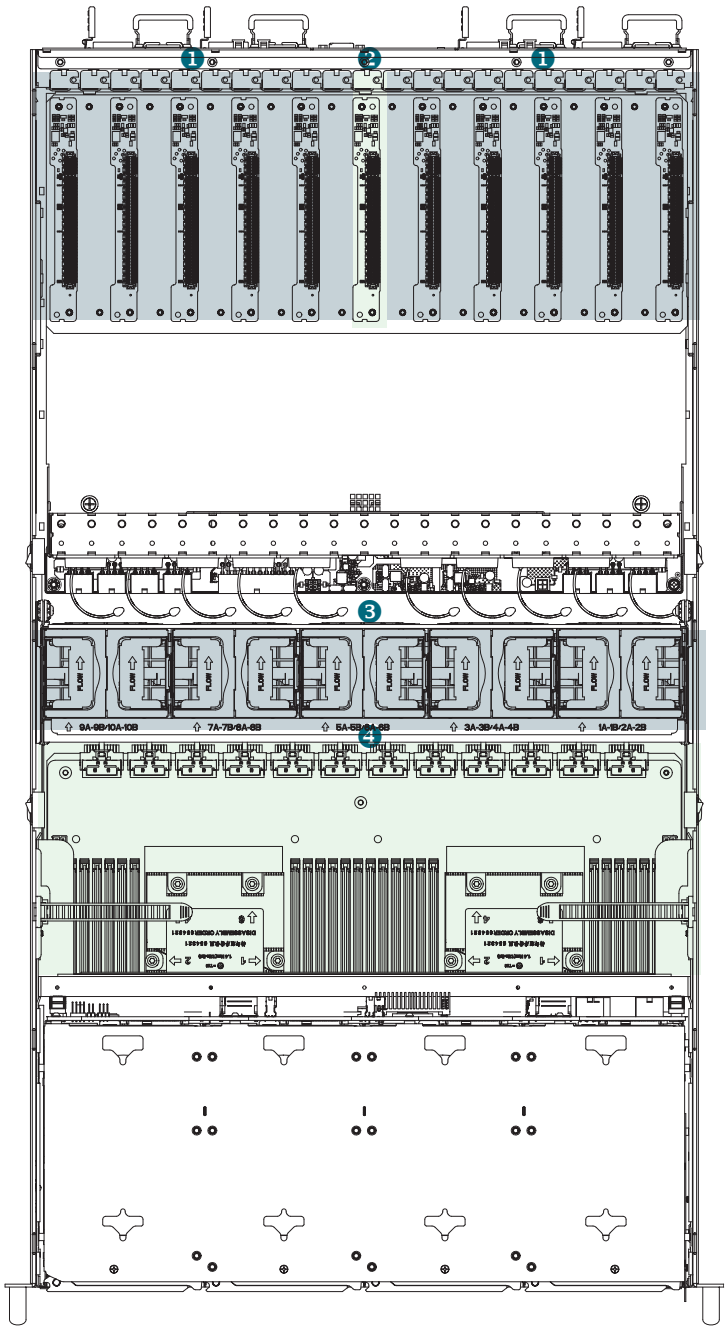
Item	Description
1	1 x Power Button+Power LED
2	1 x System Reset Button
3	1 x System ID Button
4	1 x Com Port
5	2 x USB 3.2 Gen1x1 Type A in double-stack connector
6	1 x RJ45 10GbE LAN Port
7	1 x RJ45 10GbE LAN Port
8	1 x GbE RJ45 dedicated to BMC management port
9	1 x external DB-15 VGA port
10	1 x Displayport

Rear Panel



Item	Description
1	Up to 9600W (3+1 3200W modules) redundant power supply 80+ Titanium
2	8x PCIe x 16 FHFL/ dual slot
3	1x PCIe x 16 FHFL
4	1 x DB-15 VGA connector 1 x RJ45 1GbE connectors 2 x USB 3.0 Type-A connectors 1 x COM connector (Audio Jack)

Top View



Item	Description
1	8x PCIe x 16 FHFL (dual slot)
2	1x PCIe x 16 FHFL
3	10x 80x56 hot swap fans
4	1 x Norma Motherboard

Chapter 2. Hardware Setup

This chapter provides the graphic detail and basic instruction for hardware installation. Turn off the system and unplug all peripheral devices before proceeding.

2.1 Central Processing Unit

The serverboard supports Dual AMD EPYC™ 9004/9005-series processor and Socket SP5 (LGA 6096)

2.1.1 Installation

To ensure a safe and easy setup, you need to prepare before installation:

☑ a T20 Torx screwdriver

☑ ESD wrist strap/mat and conductive foam pad

☑ Safe and stable environment

CAUTION

The pins of the processor socket are vulnerable and easily susceptible to damage if fingers or any foreign objects are pressed against them. Please keep the socket protective cover on when the processor is not installed.

CAUTION

When unpacking a processor, hold the processor only by its edges to avoid touching the contacts.

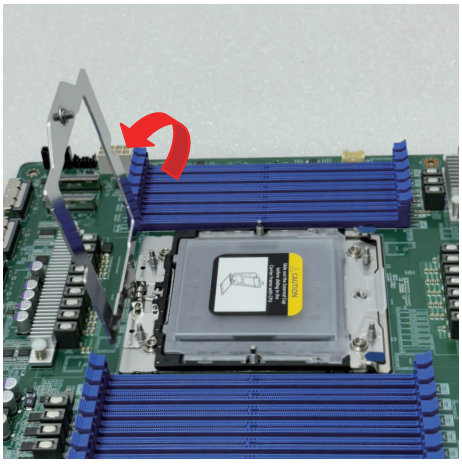
Assembly of Package and Heatsink
Procesures:

Step 1: Open the captive screw and Retention Frame
① Use T-20 6-Lobe to loosen the captive screw and away from the Retention Frame.
② Loosen the captive screw the Retention Frame will automatically pump up.

❶

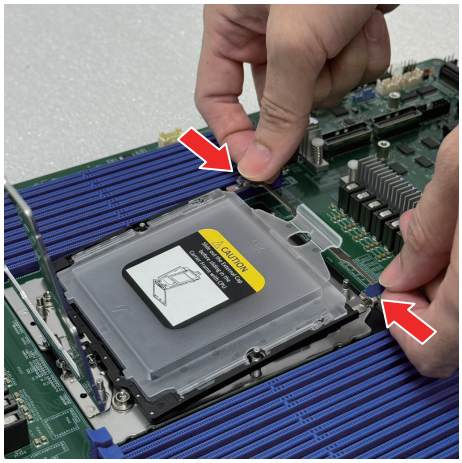


❷

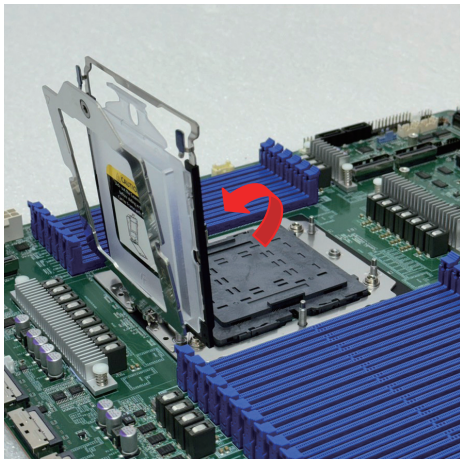


Step 2: Bounce the Rail Frame
① Use your the index finger the both hands placed on Rail Frame both sides of the metal handle.
② Then rotate Rail frame to fully open position.

❶



❷



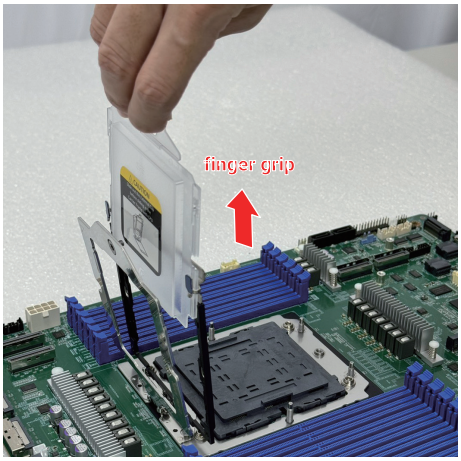
This information is provided for professional technicians only.

Step 3: Insert the package

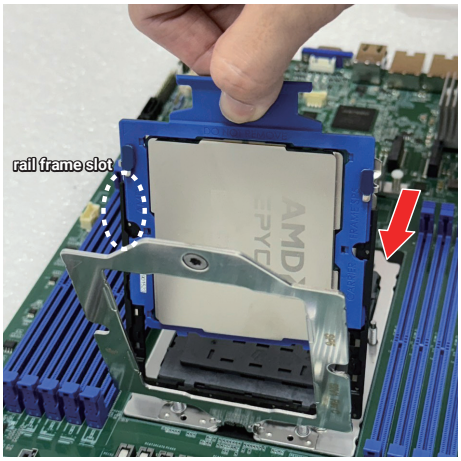
① Hold the Rail Frame, then remove the External Cap.

② Insert the Carrier Frame with package to the Rail Frame slot by holding the finger grip.

❶



❷



- Do not touch the package pad.
- Carrier Frame should slide into Rail Frame slot when insert the Package.

CAUTION

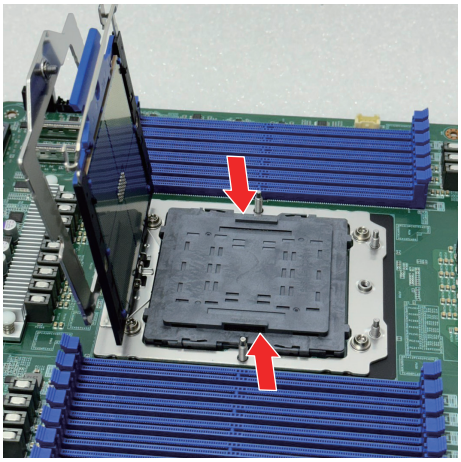
Be sure Carrier Frame with Package may be drop off if Frame did not fix by Rail Frame slot. Make sure carrier frame will slightly “click” with rail frame. Carrier Frame drop off will damage socket cap & contact.

Step 4: Remove PnP Cap

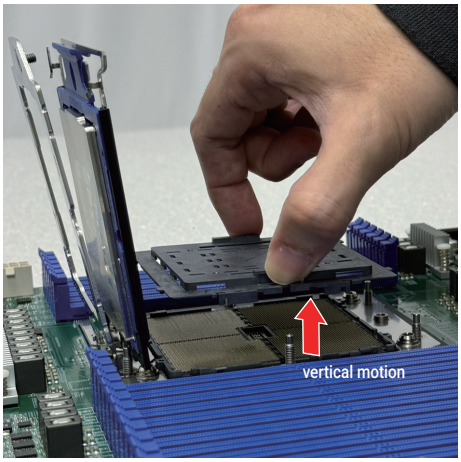
① Grip the two lift tabs marked "REMOVE" at the middle of the long sides of the PnP Cover Cap.

② Carefully remove the PnP Cap in a vertical motion only.

❶



❷



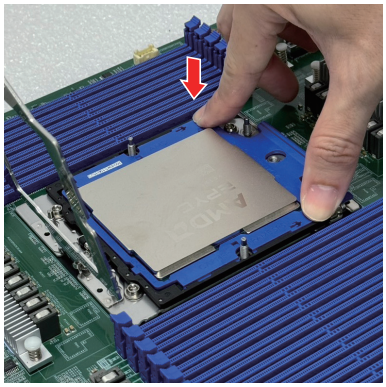
Step 5: Assembly Package and Heatsink Operation Guide

① Use the finger of two hands to press the Rail Frame with package on Stiffener Frame. Slightly press down with “click” feeling.

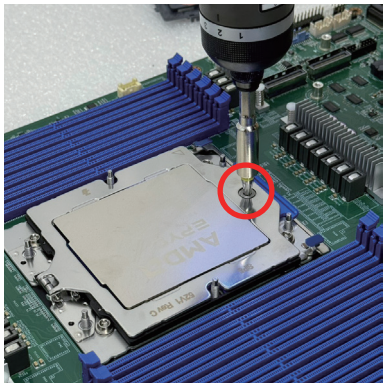
② Press Retention Frame and then tighten the captive screw.

③ Final status of whole assembly process.

❶



❷



❸



- Be care that Carrier Frame drop off with abnormal operation, Socket contact will been damaged.
- Torque : 12.5-15kgf cm

Step 6: Loading the Heatsink

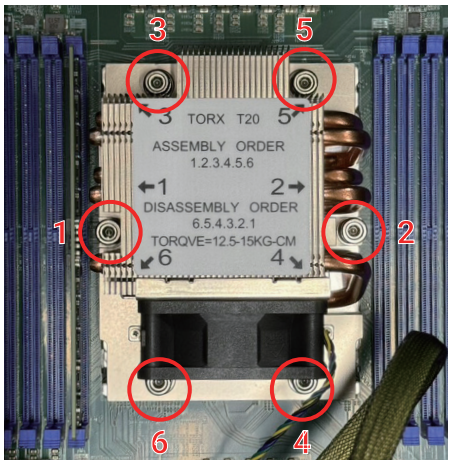
① Align the Heatsink with 4 screws on Stiffener Frame and 2 screws on Back Plate.

② Use T20 6 Lobe driver tighten 6 Heatsink nuts in sequence as 1 to 6.

❶



❷



- Torque : 12.5-15kgf cm
- When tightening 6 Heatsink nuts, we need to pre-tighten the nuts instead of completely tightening them, and we need to balance the Heatsink as much as possible.

2.2 System Memory

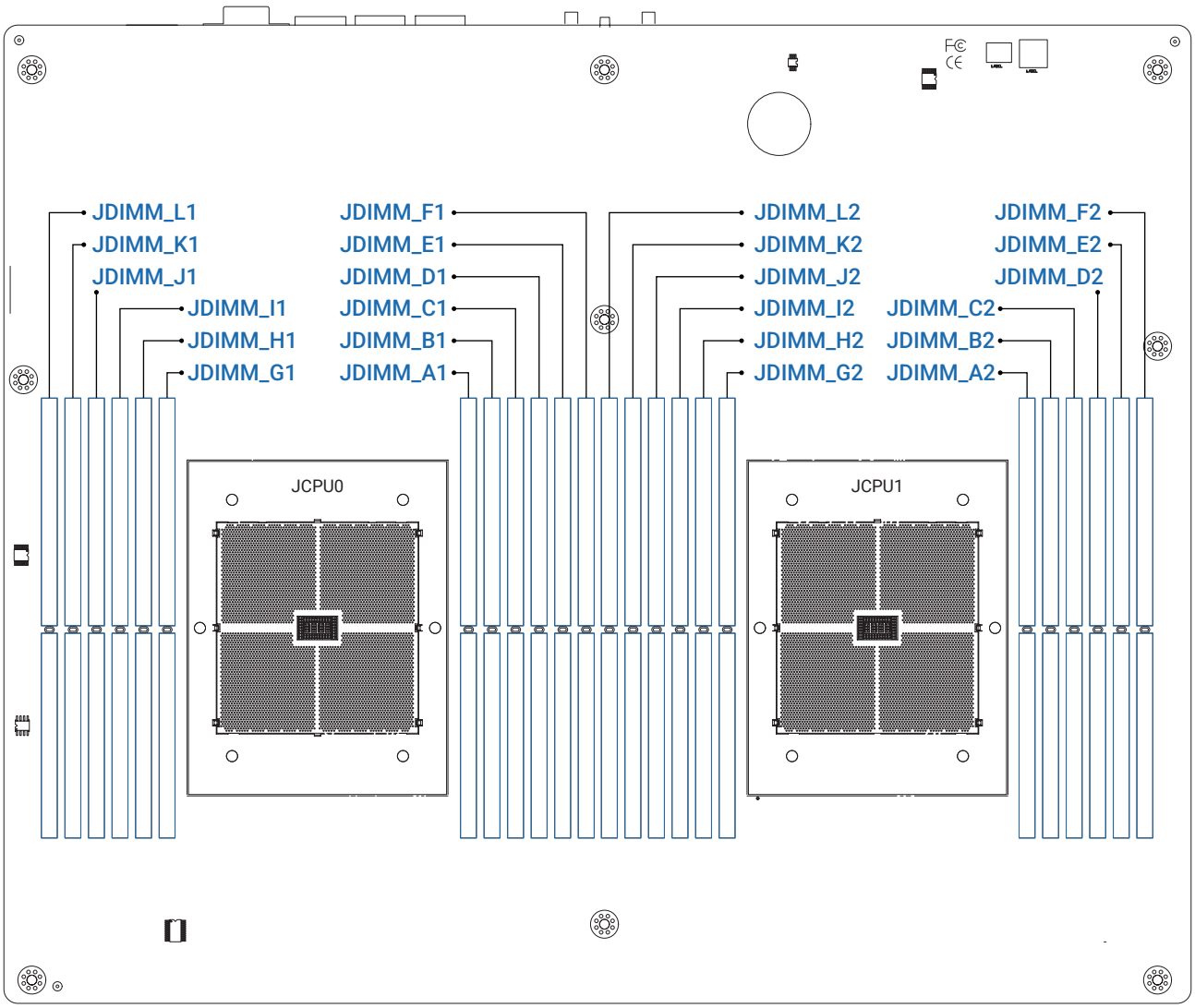
2.2.1 Placement

The DIMMs are displayed on the Norma board as JDIMM_A1/JDIMM_B1/JDIMM_C1/JDIMM_D1/JDIMM_E1/JDIMM_F1/JDIMM_G1/JDIMM_H1/JDIMM_I1/JDIMM_J1/JDIMM_K1/JDIMM_L1/JDIMM_A2/JDIMM_B2/JDIMM_C2/JDIMM_D2/JDIMM_E2/JDIMM_F2/JDIMM_G2/JDIMM_H2/JDIMM_I2/JDIMM_J2/JDIMM_K2/JDIMM_L2

To ensure satisfactory performance, you need to:

☑ Verify the DIMM type:
This product supports DDR5 RDIMM

☑ Verify if all of the DIMMs installed are of the same DIMM type to avoid memory failure and loss of performance speed.



2.2.2 DIMM Population

NOTE

Rules to abide by before installation:

- Must install at least one DDR5 DIMM per socket.

The symbol # in the graph below indicates that the DIMM slot is populated.

1 CPU Configuration

Placement		DIMM Number						
		1	2	4	6	8	10	12
CPU0	JDIMM_A1	#	#	#	#	#	#	#
	JDIMM_B1				#	#	#	#
	JDIMM_C1			#	#	#	#	#
	JDIMM_D1						#	#
	JDIMM_E1					#	#	#
	JDIMM_F1							#
	JDIMM_G1		#	#	#	#	#	#
	JDIMM_H1				#	#	#	#
	JDIMM_I1			#	#	#	#	#
	JDIMM_J1						#	#
	JDIMM_K1					#	#	#
	JDIMM_L1							#

2 CPU Configuration

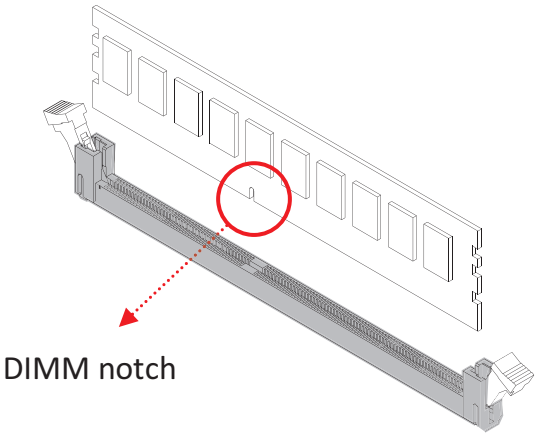
Placement		DIMM Number						
		1	2	4	6	8	10	12
CPU0	JDIMM_A1	#	#	#	#	#	#	#
	JDIMM_B1				#	#	#	#
	JDIMM_C1			#	#	#	#	#
	JDIMM_D1						#	#
	JDIMM_E1					#	#	#
	JDIMM_F1							#
	JDIMM_G1		#	#	#	#	#	#
	JDIMM_H1				#	#	#	#
	JDIMM_I1			#	#	#	#	#
	JDIMM_J1						#	#
	JDIMM_K1					#	#	#
	JDIMM_L1							#
Placement		1	2	4	6	8	10	12
CPU1	JDIMM_A2	#	#	#	#	#	#	#
	JDIMM_B2				#	#	#	#
	JDIMM_C2			#	#	#	#	#
	JDIMM_D2						#	#
	JDIMM_E2					#	#	#
	JDIMM_F2							#
	JDIMM_G2		#	#	#	#	#	#
	JDIMM_H2				#	#	#	#
	JDIMM_I2			#	#	#	#	#
	JDIMM_J2						#	#
	JDIMM_K2					#	#	#
	JDIMM_L2							#

2.2.3 Installation

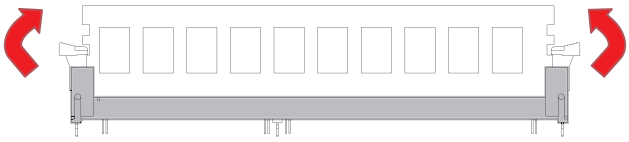
Step 1 Unlock the DIMM socket by pressing the retaining clip outward.



Step 2 Insert the memory module into the slot. Make sure that the DIMM notch is accurately positioned.



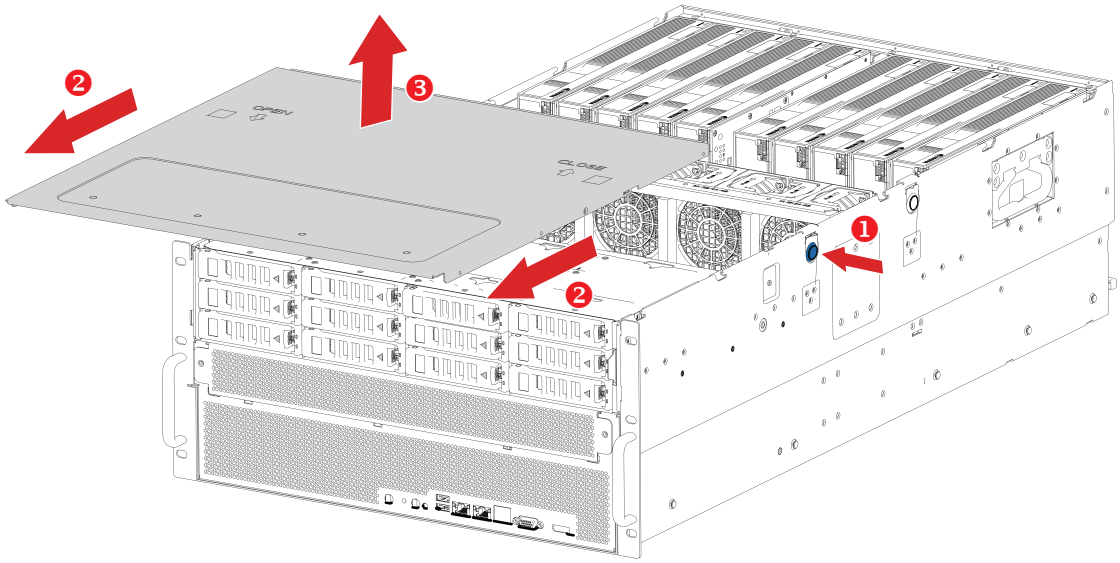
Step 3 Close the retaining clip to complete installation.



2.3 Top Cover

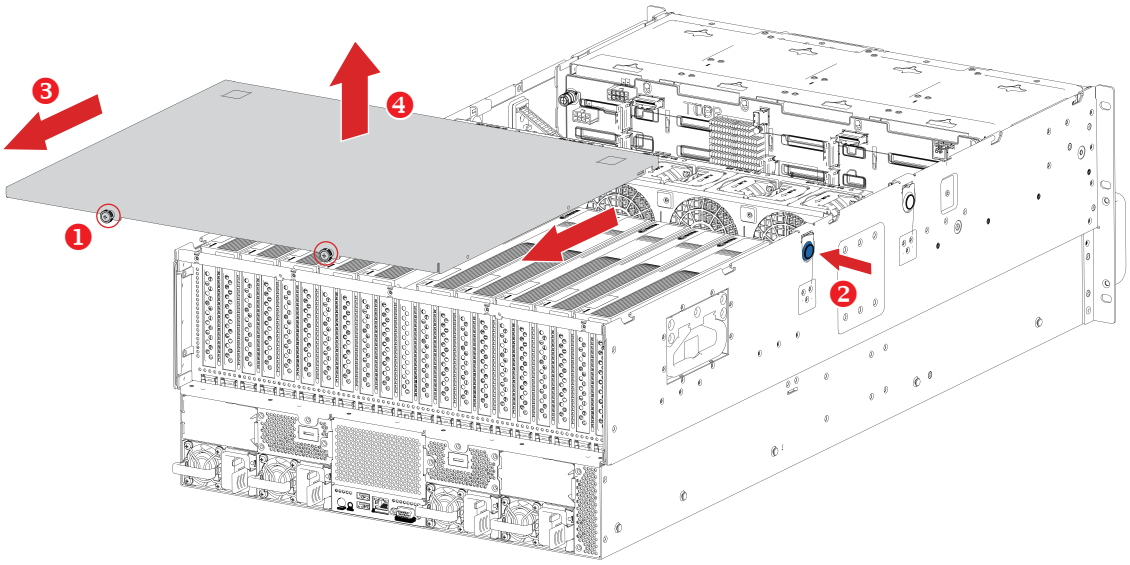
Front Top Cover

① Press the release button on both sides of the chassis.
② Slide the top cover towards the front panel.
③ Lift the top cover upward to remove.



Rear Top Cover

① Lossen the captive screws on the rear side.
② Press the release button on both sides of the chassis.
③ Slide the top cover towards the rear panel.
④ Lift the top cover upward to remove.

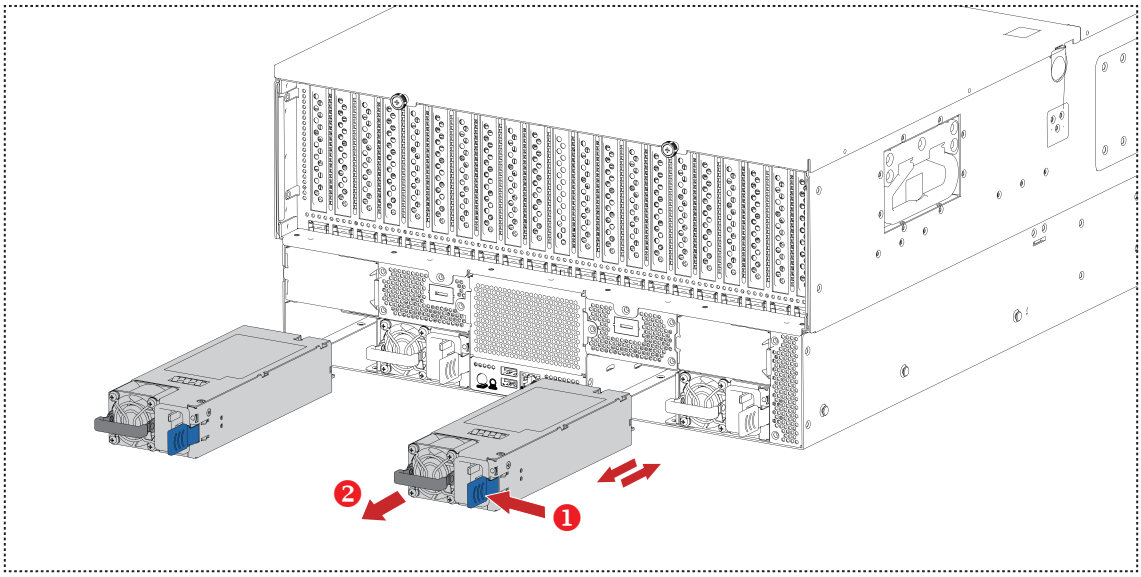


This information is provided for professional technicians only.

2.4 Power Supply Unit

2.4.1 Installation

① Press the ejector to release the module.
② Pull the handle to remove the module out of the chassis.
③ Push the replaced power supply unit into the chassis. Ensure that the module is hooked into the cage.



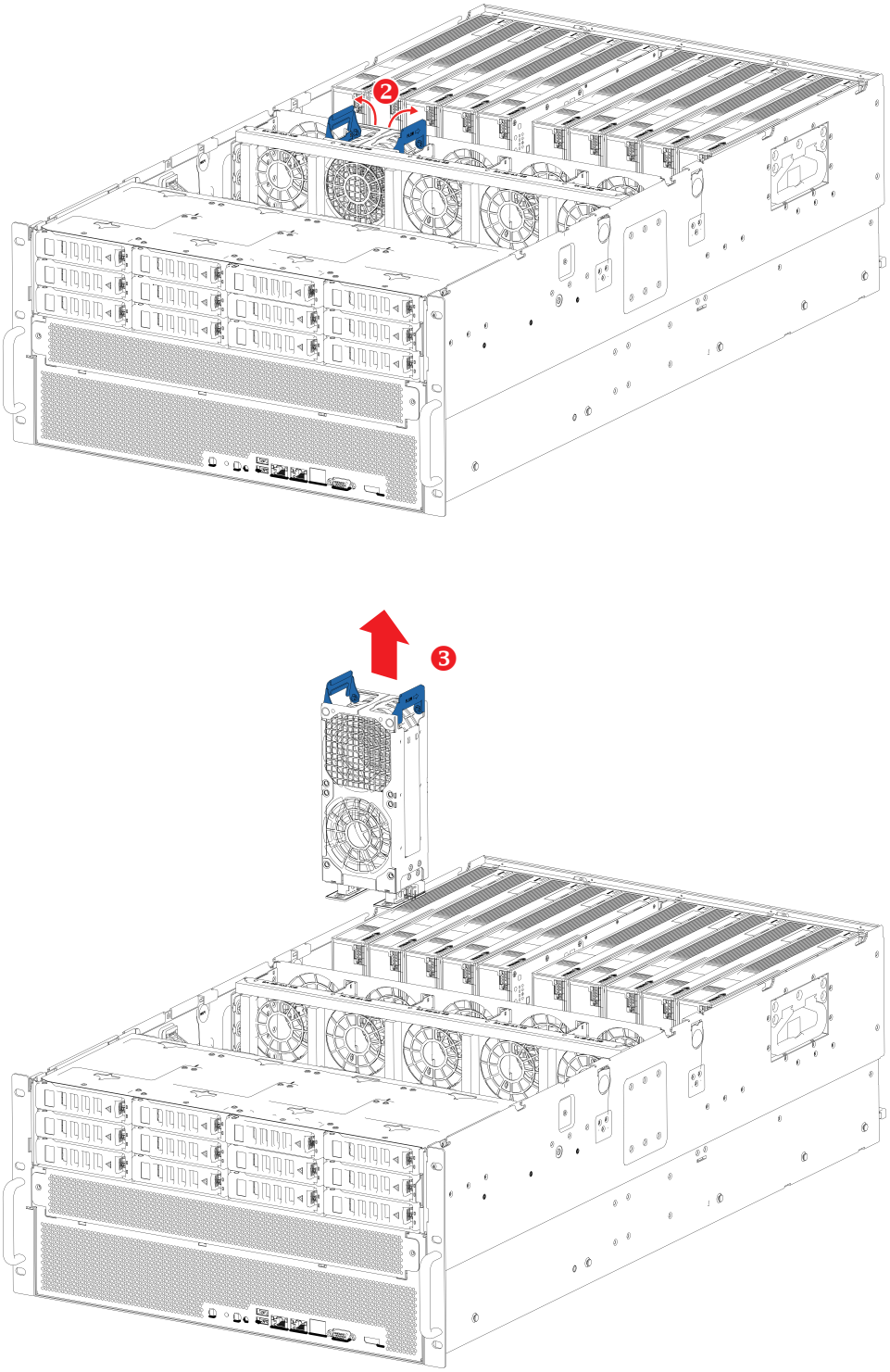
2.4.2 LED Indicator

Color	Behavior	Description
Green	Solid	Output on and working normally.
	Blinking, 1Hz	AC present/ only 12Vsb (PS off) or PSU is in cold redundant state.
	Blinking, 2Hz	Power supply FW updating.
Amber	Solid	AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.
	Solid	Power supply critical event causing a shutdown; AC cord unplugged or AC power lost, failure, OCP, OVP, fan fail.
	Blinking, 1Hz	Power supply warning events where the power supply continues to operate high temp, high power, high current, slow fan.

This information is provided for professional technicians only.

2.5 Fan

① Remove the top cover from the chassis. Please refer to Section 2.3 Top Cover.
② Flip the fan handles (marked in blue as demonstrated) and hold the fan module on the both side.
③ Unplug the fan cables and connectors from the server board and pull the fan upward to remove it.

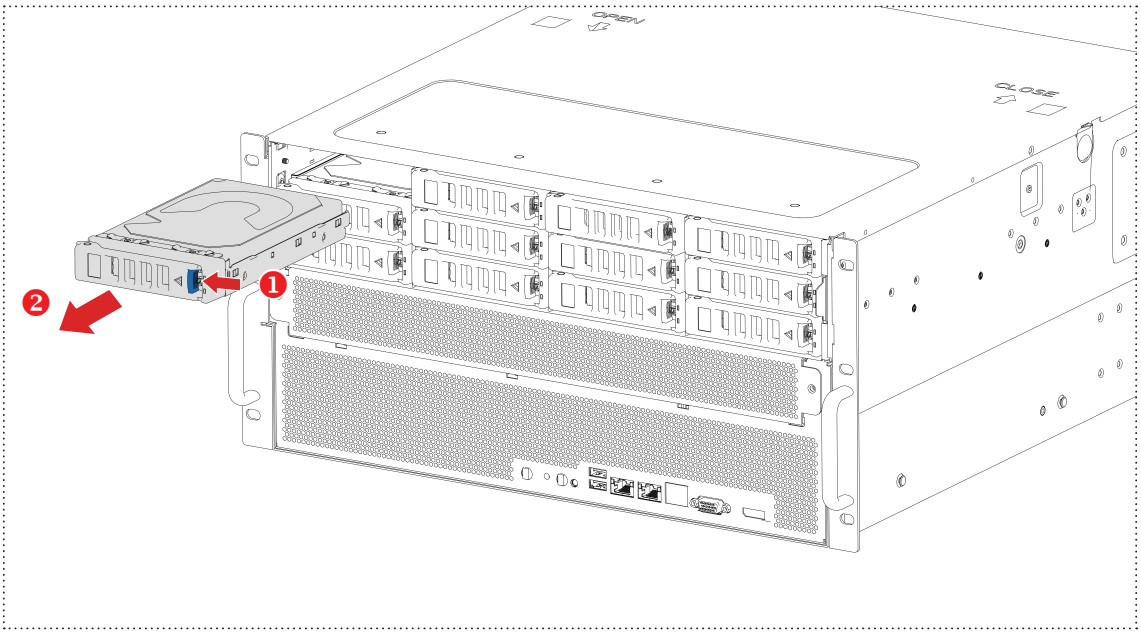


⚠ Please turn off the power before removing the fans.

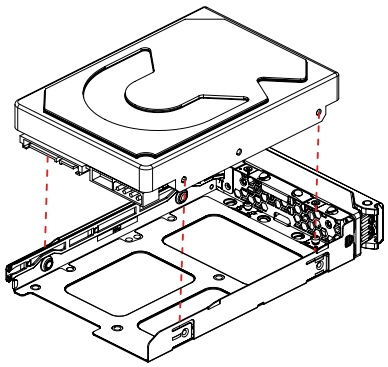
2.6 Disk Drive

2.6.1 Disk Drive: 3.5-inch

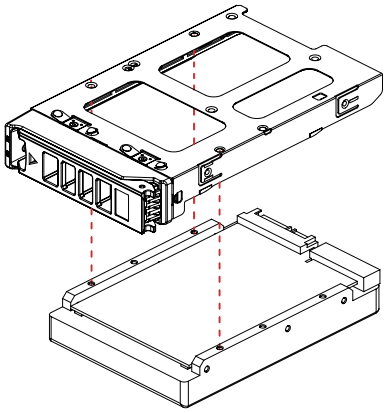
① Press the ejector on the tray to release the handle.
② Pull the tray handle completely outward.
③ Pull the drive tray out of the chassis.



④ Insert the disk drive into the tray. Ensure that the dimples on the tray match the disk drive. For additional assurance, fasten the screws * 2 on the tray to secure the disk drive.



dimple placement



screw placement

⑤ Push the tray with the installed disk drive into the end of the drive slot in the chassis.
⑥ Close the tray handle.

This information is provided for professional technicians only.

2.6.3 LED Indicator

SATA

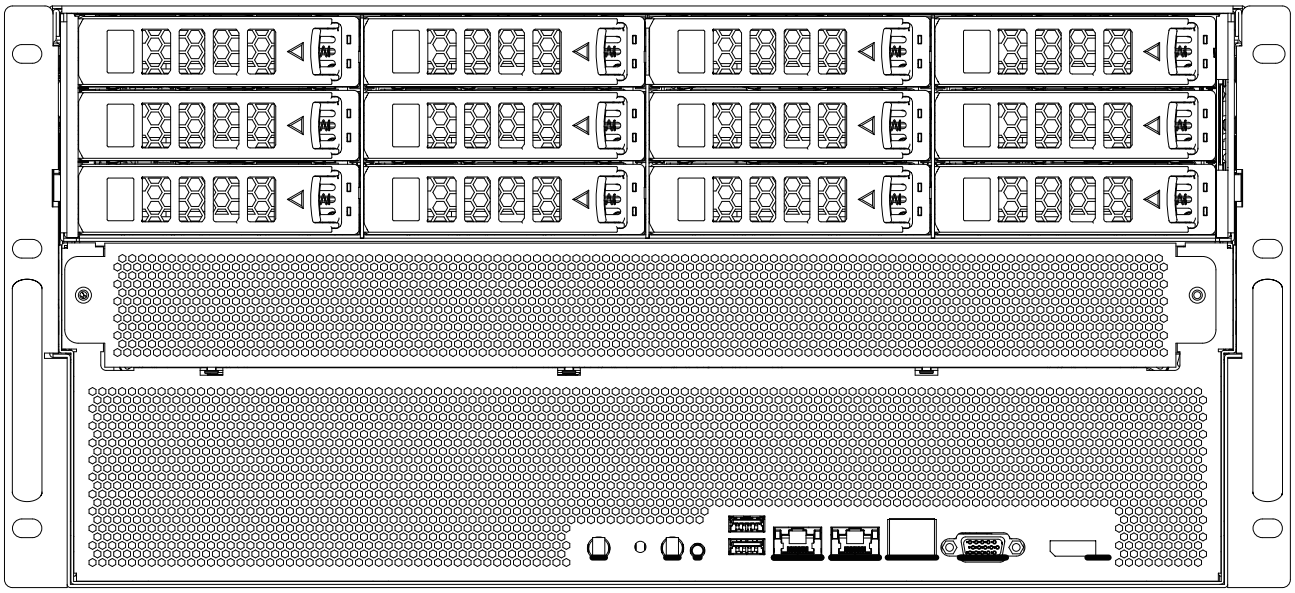
Indicator	Color	Behavior	Description
HDD Activity	Blue	On	HDD is present.
		Blinking	HDD Activity is detected or Locate HDD.
	---	Off	HDD is not connected or the system power is off.
HDD Fail/Staus LEDs	Red	On	HDD Fault or Locate HDD
		Blinking	Re-build status
	---	Off	Normal

NVMe

Indicator	Color	Behavior	Description
HDD Activity	Blue	On	HDD is present.
		Blinking	HDD Activity is detected.
	---	Off	HDD is not connected or the system power is off.
HDD Locate LEDs	Green	On	HDD is located.
	---	Off	----
HDD Fail LEDs	Red	On	HDD Fault
	---	Off	Normal

2.6.4 Drive Slot Map

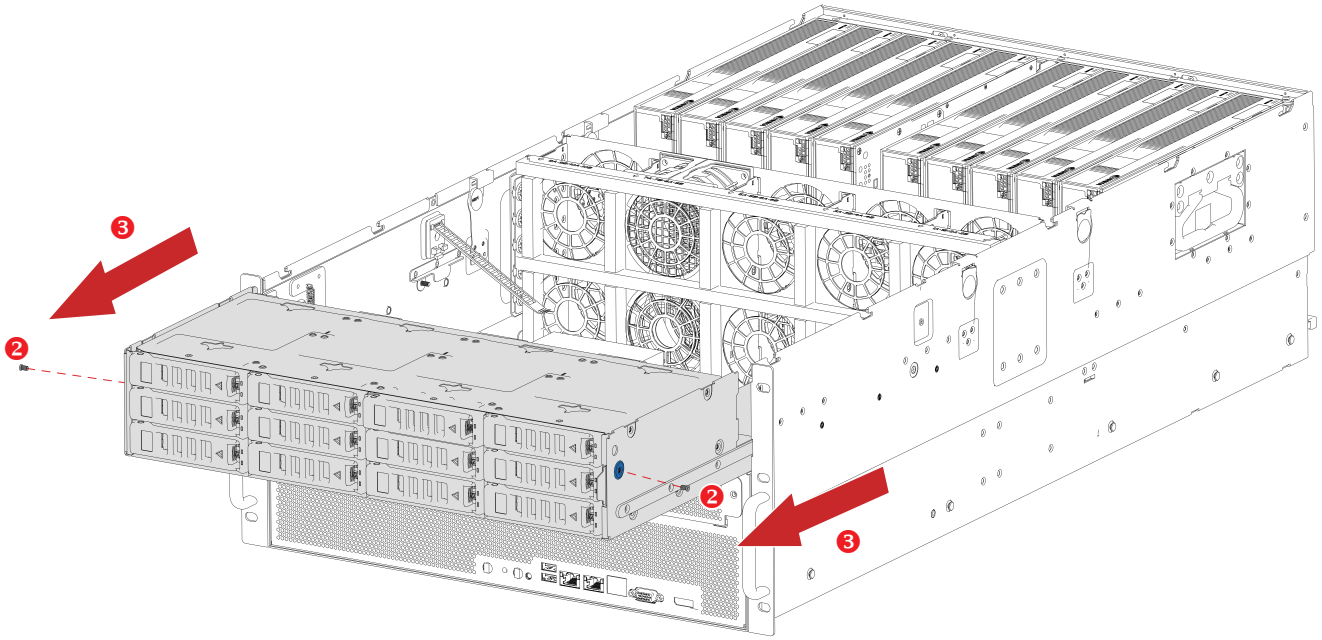
Front Panel with Disk drive



Drive Slot Number			
NVMe 1	NVMe 2	NVMe 3	NVMe 4
SATA/SAS 1	SATA/SAS 2	SATA/SAS 3	SATA/SAS 4
SATA/SAS 5	SATA/SAS 6	SATA/SAS 7	SATA/SAS 8

2.7 HDD Tray

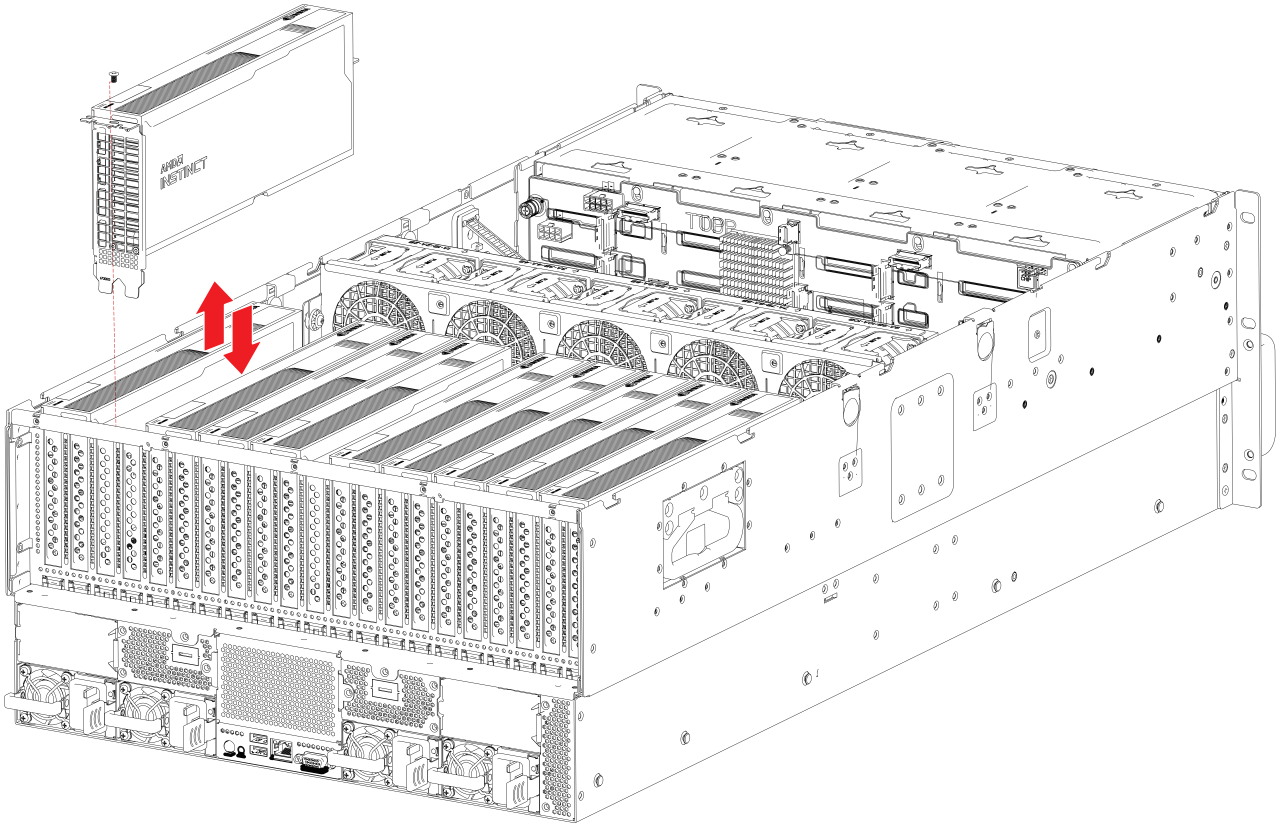
① Remove the front top cover from the chassis. Please refer to Section 2.3 Top Cover.
② Dislodge the screws*2 on the both side of the chassis.
③ Simutaneously pull the HDD tray outward.



This information is provided for professional technicians only.

2.8 GPU Card

① Remove the rear top cover from the chassis. Please refer to Section 2.3 Top Cover.
② Properly align the GPU card with the slot and press down the GPU card.
③ Fasten the screw to firmly install the GPU card.

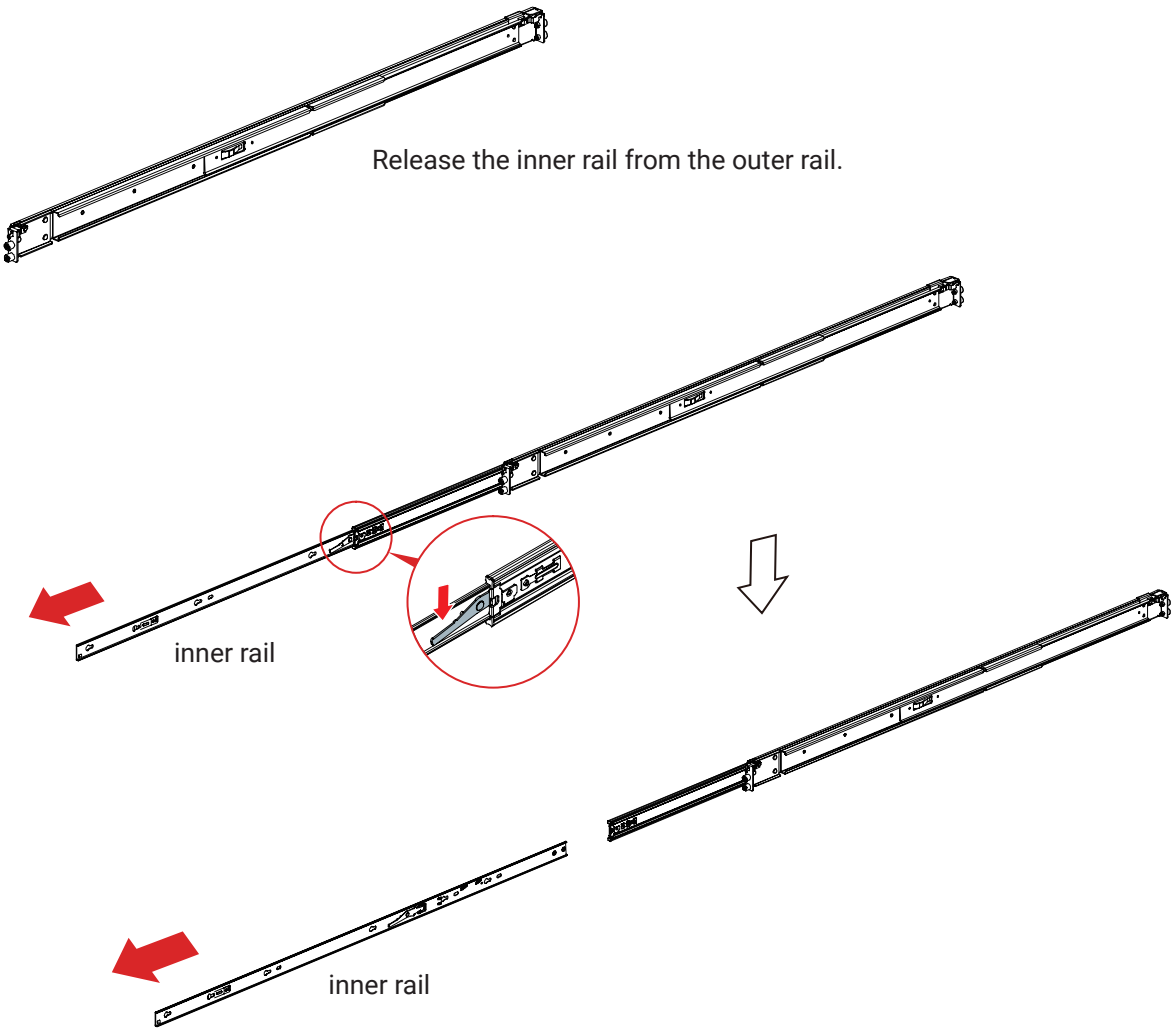


2.9 Slide Rail

NOTE
This section provides a basic instruction for mounting the slide rail onto the system. Tool-less rails vary per order. The rail in this manual may not exactly match the rail for your system. Please refer to the specifications or quick installation guide that came with your purchased product.

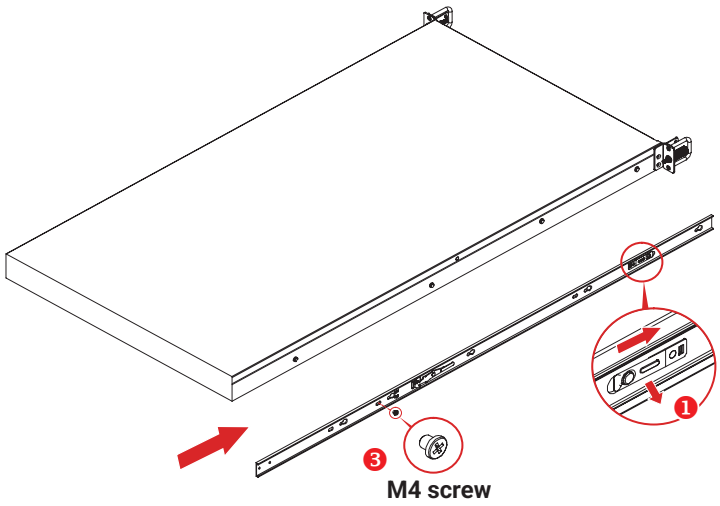
CAUTION
The rack may tilt and fall due to incorrect installation or placed on uneven grounds. The rack must be placed in a flat surface before you begin to slide the system barebone in for servicing.

Release the inner rail form the outer rail
1. Extend the inner rail until it stops.
2. Press the release lever on the inner rail to remove it from the outer rail.



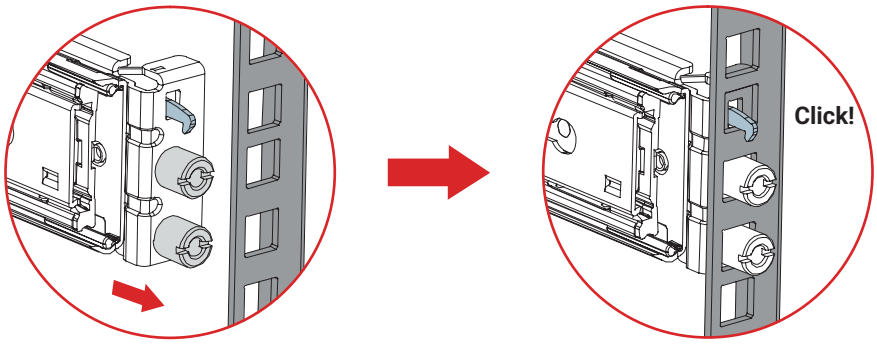
Install the inner rail onto the chassis

1. Press the release rail against the chassis and lift the clip.
2. Slide the inner rail toward the chassis rear.
3. Tighten the rail screws onto the chassis.



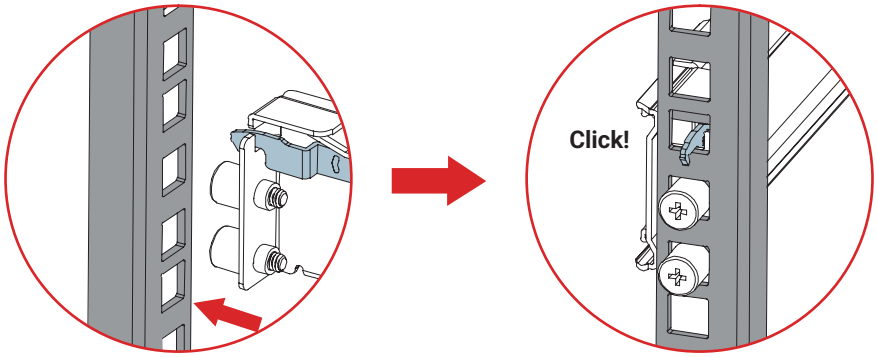
Attach the outer rail onto the rack

1. Align the rack mount pins (studs) with the rack posts, lift the lever, and push forward.



Rear Bracket

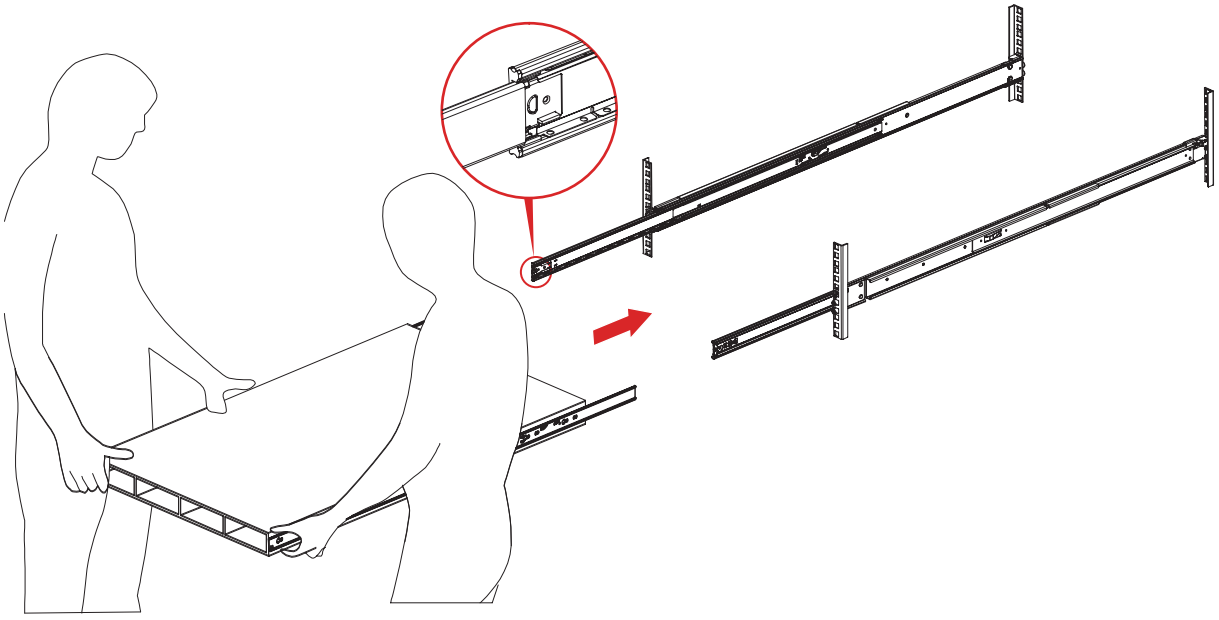
2. Align the rack mount pins (studs) with the rack posts, lift the lever, and pull back until it clicks.



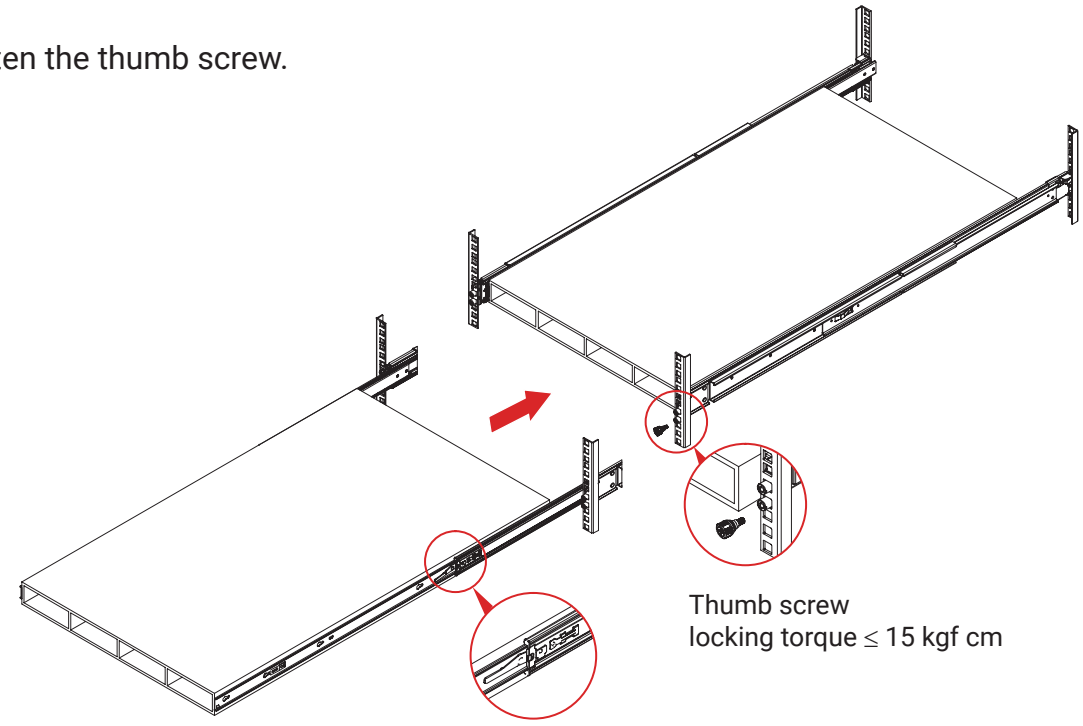
Front Bracket

Insert the chassis to completed the installation

1. Pull the middle rail fully extended in lock position, ensure ball bearing retainer is located at the front of the middle rail.
2. Horizontally insert the chassis into middle-outer rails.



3. Fasten the thumb screw.



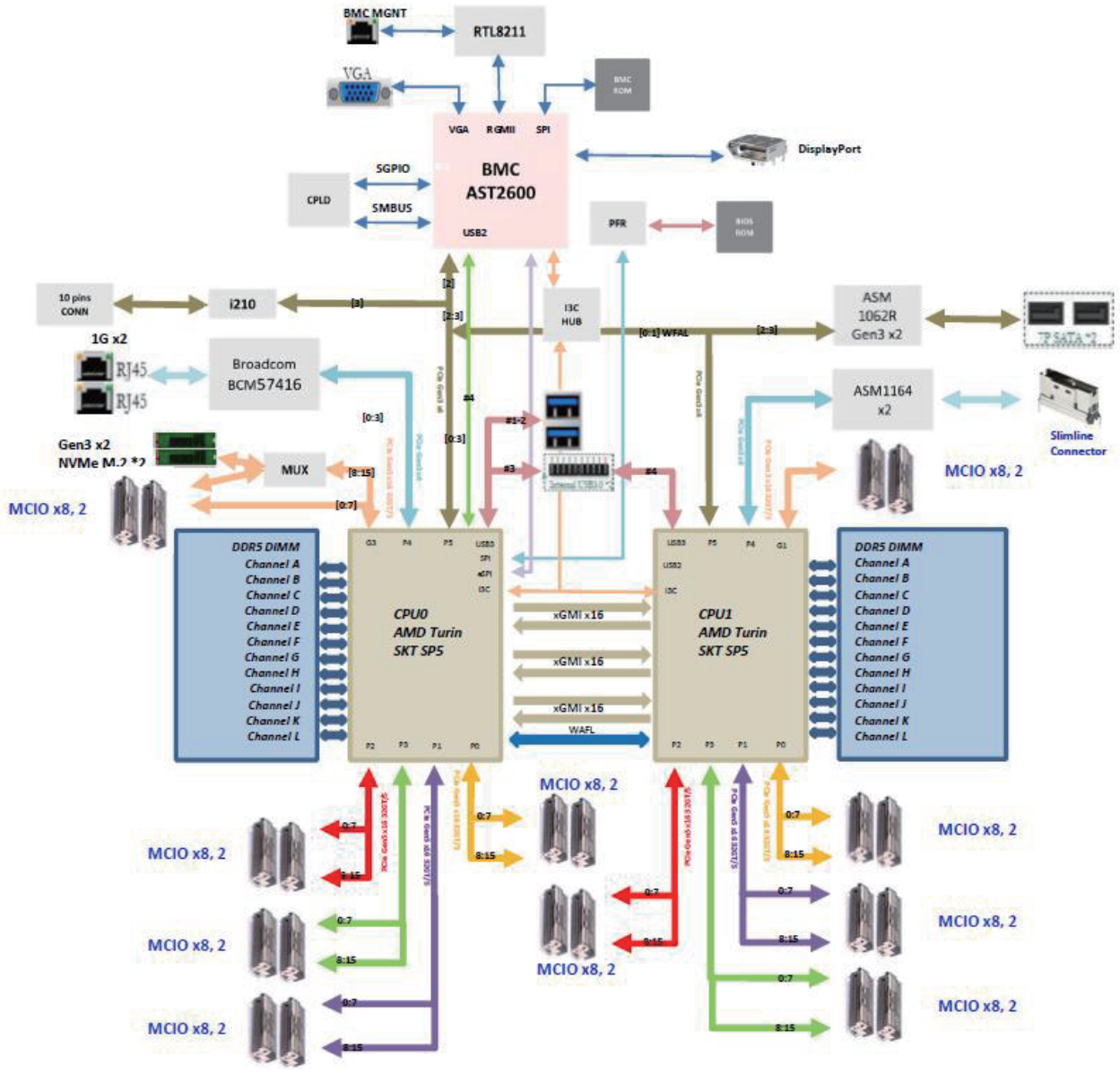
Thumb screw
locking torque ≤ 15 kgf cm

This information is provided for professional technicians only.

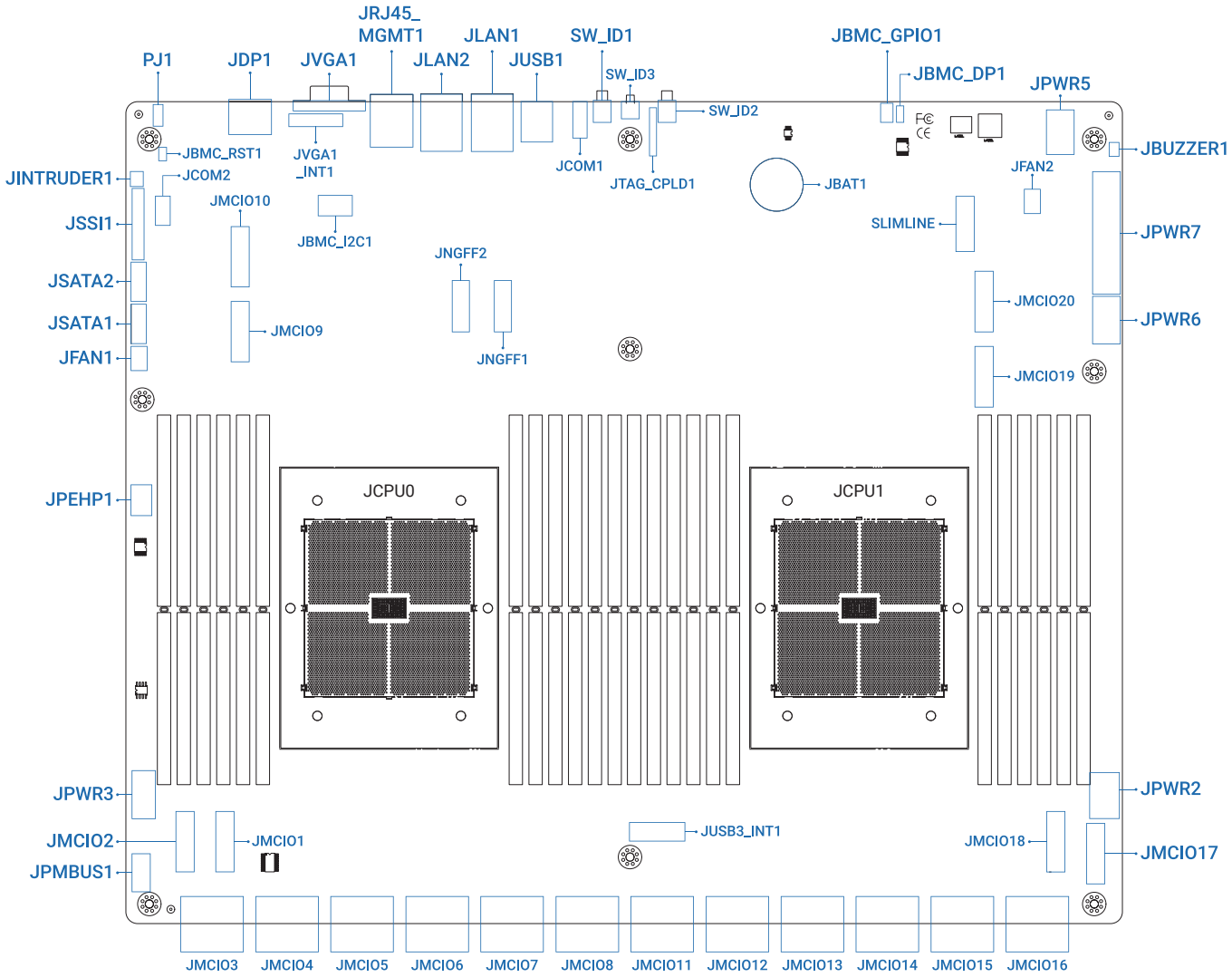
Chapter 3. Hardware Settings

This section provides illustrations that display the internal jumpers, connectors, and system LED indicators on the Norma motherboard. The motherboard layout and essential connectors are listed below for your reference.

3.1 Block Diagram



3.2 Placement



3.3 Content List

External Connectors - Rear I/O

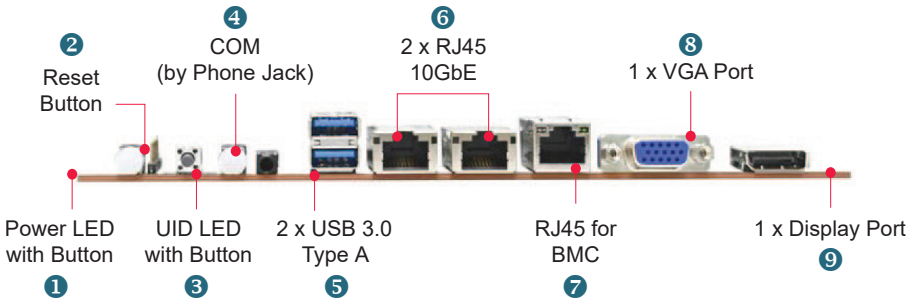
Function	Description	Comments
Ethernet x2	RJ45	JLAN1, JLAN2:10G/1G NIC (Broadcom BCM57416)
VGA	DSUB 15 Pin Blue Female	JVGA1
USB3.0 x2	USB3.0 Type A	JUSB1
Ethernet x1	RJ45	JRJ45_0:10/100/1000M PHYCEIVER (RTL8211FS)
Display port	Display port	JDP1
SERIAL PORT	Phone Jack	JCOM1

Internal Connectors Summary

Function	Description	Comments
Power Supply	12 x 2 Pin ATX CONN	JPWR7:12V, 5V, 3.3V, 5VSB
Power Supply	4 x 2 Pin ATX CONN	JPWR1, JPWR2, JPWR3, JPWR5, JPWR6:12V
CPU	SP5 LGA6096	JCPU0, JCPU1
Front Panel	12 x 2 Pin 2.54mm Box Header	JSSI1
Front USB(3.0)	10 x 2 Pin 2.0mm Box Header	JUSB3_INT1
Front USB(2.0)	5 x 2 Pin 2.0mm Header	JUSB2_INT2
BMC GPIO	3 x 2 Pin 2.0mm Box Header	JBMC_GPIO1
FAN CONN	4 x 1 Pin 2.54mm Box Header	JFAN1, JFAN2
PCIE Hot-Plug SMB	4 x 2 pin 2.0mm Box Header	JPEHP1
PMBUS	5 x 1 Pin 2.54mm Box Header	JPMBUS1
BMC Debug Port	3 x 1 Pin 2.00mm Header	JBMC_DP1
BMC Buzzer	2 x 1 Pin 2.54mm Header	JBUZZER1
PFR Module	GEN4_M2_KEY_M_H=8.5MM	JPFR1
Intruder	2 x 1 Pin 2.0mm Box Header	JINTRUDER1
M.2 2280	GEN5_M2_KEY_M_H=8.5MM	JNGFF1、JNGFF2
BMC Reset	2 x 1 Pin 2.0mm Header	JBMC_RST1
Program CPLD FW	8 x 1 Pin 2.54mm Header	JTAG_CPLD1
VRM SMB	3 x 1 Pin 2.54mm Header	PJ1
Front Ethernet(NCSI)	10 x 2 Pin 2.0mm Box Header	JLAN3_INT1
BMC COM Port	2 x 5 Pin 2.0mm Box Header	JCOM1_INT1、JCOM2
BMC I2C	4 x 2 pin 1.25mm Box Header	JBMC_I2C1
Clear CMOS	3 Pin 2.54mm Header	JCMOS1
BMC RST PW	2 x 1 Pin 2.0mm Header	JBMC_DEFAULT1
BMC Socflash Enable	2 x 1 Pin 2.0mm Header	JSOC_FLASH1
BMC Through PFR or Bypass	2 x 1 Pin 2.0mm Header	JBMC_MUX1
PMBUS Power Select	3 x 1 Pin 2.54mm Header	JPMBUS_SEL1
CPU Through PFR or Bypass	3 x 1 Pin 2.0mm Header	JBIOS_MUX1, JBIOS_MUX2
Battery Socket	2 Pin Socket	JBAT1
CPU COM Port	5 x 2 Pin 2.0mm Box Header	JUART0
BMC Disable	2 x 1 Pin 2.0mm Header	JBMC_DIS1

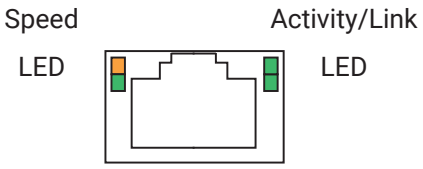
Function	Description	Comments
DIMM Sockets	287 Pin DDR5 DIMM	JEDEC Specified DDR5 Connector: JDIMM_A1~L1, JDIMM_A2~L2
BIOS SPI ROM Socket	SOIC-16 Socket	JSPI_BIOS1
BMC SPI ROM Socket	SOIC-16 Socket	JSPI_BMC1
Board SKU ID Select	2 x 1 Pin 2.0mm Header	JID_0~6
VGA	2 x 8 Pin 2.0mm Box Header	JVGA_INT1
VGA Select	2 x 1 Pin 2.0mm Header	JVGA_SEL1
BMC Force IP	2 x 1 Pin 2.0mm Header	JFORCE_IP1
BMC Clear Password	2 x 1 Pin 2.0mm Header	JCLR_PSWD1
I3C debug	3 x 1 Pin 2.0mm Header	JI3C_DBG1
I3C debug	3 x 1 Pin 2.0mm Header	JI3C_MNG1
I3C debug	3 x 1 Pin 2.0mm Header	JI3C_SPD1
I3C debug	3 x 1 Pin 2.0mm Header	JI3C_SPD2
I3C debug	3 x 1 Pin 2.0mm Header	JI3C_SPD3
I3C debug	3 x 1 Pin 2.0mm Header	JI3C_SPD4
CPLD PWR ON	2 x 1 Pin 2.0mm Header	JPWR_ALL1
PWR button for debug	2 x 1 Pin 2.0mm Header	JPWR_SW_INT1
HDT CONN	Samtec 10 x 2 Pin CONN	JHDT1
PCIE MUX I2C CONN	3 x 1 Pin 2.54mm Header	J1
JTAG EN	2 x 1 Pin 2.0mm Header	J2
Serial ATA	7 Pin 1.27 mm Headers	JSATA1, JSATA2
SLIMLINE(SATA)	Slimline 8i (SFF-8654) CONN	SASHD_P1

3.4 External Port



Item	Description
1	Power LED with Button
2	Reset Button
3	UID LED with Button
4	COM (by Phone Jack)
5	2 x USB 3.0 Type A
6	2 x RJ45 10GbE
7	RJ45 for BMC
8	1 x VGA Port
9	1 x Display Port

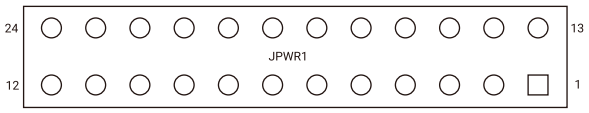
BMC Management RJ45 LED Indicator



Item	Color	Behavior
Activity/Link LED	Green (blinking)	Activity detected.
	Off	Not active, LAN cable no connect.
	On	Link.
Speed LED	Off	10M bps connection or no link.
	Green	100M bps connection.
	Orange	1G bps connection.

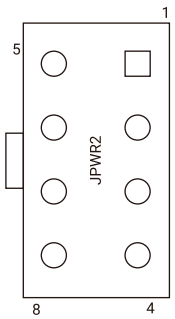
3.5 Connector Definition

Power Supply Connector (JPWR7)
This is a 2x12-pin connector that provides the motherboard with power.



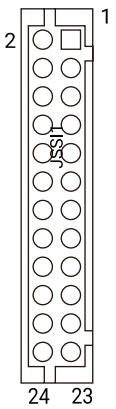
P3V3	13	1	P3V3
N.C.	14	2	P3V3
GND	15	3	GND
PSU_PSON_BUF_N	16	4	P5V_PSU
GND	17	5	GND
GND	18	6	P5V_PSU
GND	19	7	GND
N.C.	20	8	PSU_PWROK
P5V_PSU	21	9	P5V_STBY_PSU
P5V_PSU	22	10	P12V_PSU
P5V_PSU	23	11	P12V_PSU
GND	24	12	P3V3

Power Supply Connector (JPWR2、JPWR3、JPWR5、JPWR6)
This is a 2x4-pin connector that provides the motherboard with power.



P12V_PSU	5	1	GND
P12V_PSU	6	2	GND
P12V_PSU	7	3	GND
P12V_PSU	8	4	GND

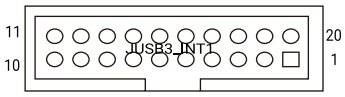
LED/Bezel Button Header (JSSI1)
This connector is a 2 x 23 Pin header.



P3V3_AUX	2	1	FP_HDR_PWR_LED
P5V_STBY_PSU	4	3	NC
ID_LED_OUT_N	6	5	FP_PWR_LED_L
SYS_HEALTH2#	8	7	HDD_LED_P
SYS_HEALTH#	10	9	HDD_LED_N
LAN1_ACTLED_PWR	12	11	FP_PWR_BTN_N
LAN1_ACTLED_N	14	13	GND
SMBUS_SDA	16	15	FP_RST_BTN_N
SMBUS_SCL	18	17	GND
CHASSIS_OPEN	20	19	BMC_ID_IN_N
LAN 2_ACTLED_PWR	22	21	P3V3_AUX
LAN2 _ACTLED_N	24	23	FP_NMI_BTN_N

Front I/O USB Header (JUSB3_INT1)

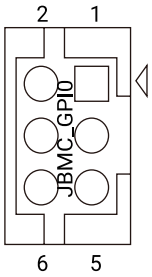
This is a 19-pin header that is used to provide front I/O USB functionality.



		1	P5V_USB23
P5V_USB23	19	2	USB3_HUB_RX_R_DN2
USB3_HUB_RX_R_DN1	18	3	USB3_HUB_RX_R_DP2
USB3_HUB_RX_R_DP1	17	4	GND
GND	16	5	USB3_HUB_TX_R_DN2
USB3_HUB_TX_R_DN1	15	6	USB3_HUB_TX_R_DP2
USB3_HUB_TX_R_DP1	14	7	GND
GND	13	8	USB2_HUB_R_DN2
USB2_HUB_R_DN1	12	9	USB2_HUB_R_DP2
USB2_HUB_R_DP1	11	10	USB_HUB_OCI2_N(NC)

BMC GPIO header (JBMC_GPIO1)

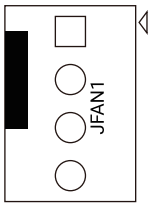
This is a 2x3-pin header that is used to provide BMC GPIO functionality.



RACK_EXTRST_N	2	1	GND
BMC_GPY1	4	3	BMC_I2C_16_SDA
BMC_GPY0	6	5	BMC_I2C_16_SCL

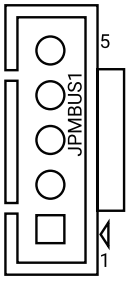
Fan Header (JFAN1~JFAN2)

This is a 1x4-pin header that is used to provide FAN functionality.



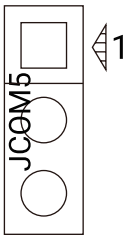
1	GND
2	P12V_FANx
3	FANx_R_TACH
4	FANx_R_PWM

PMBUS Header (JPMBUS1)
This is a 1x5-pin header that is used to provide PMBus functionality.



1	SMB_PMBUS_SCL
2	SMB_PMBUS_SDA
3	PMBUS_ALERT_N_C
4	GND
5	P5V_P3V3_AUX

BMC Debug port Header (JBMC_DP1)
This is a 1x3-pin header that is used to provide
BMC Debug port functionality.



1	SPE_TXD
2	GND
3	SPE_RXD

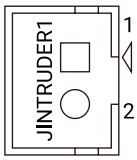
BUZZER Header (JBUZZER1)
This is a 1x3-pin header that is used to provide
BMC Debug port functionality.



1	P5V_PSU
2	BMC_BUZZER-

Chassis Intrusion header (JINTRUDER1)

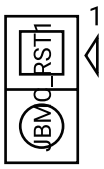
This is a 1x2-pin header that is used to provide Chassis intrusion functionality.



1	CHASSIS_OPEN
2	GND

BMC RESET header (JBMC_RST1)

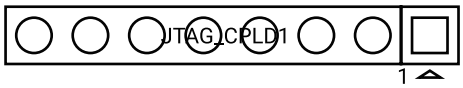
This is a 1x2-pin header that is used to provide BMC RESET functionality.



1	BMC_RESET
2	GND

CPLD JTAG header (JTAG_CPLD1)

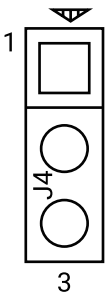
This is a 1x8-pin header that is used to provide CPLD JTAG functionality.



1	P3V3_STBY
2	JTAG_CPLD_TDO
3	JTAG_CPLD_TDI
4	PU_JTAG_CPLD_P4
5	NC
6	JTAG_CPLD_TMS
7	GND
8	JTAG_CPLD_TCK

VRM SMB header (PJ1)

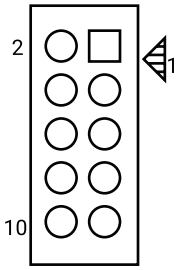
This is a 1x3-pin header that is used to provide VRM SMB functionality.



1	SMB_VR_DAT
2	GND
3	SMB_VR_CLK

BMC COM port header (JCOM1_INT1、JCOM2)

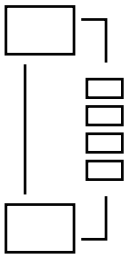
This is a 2x5-pin header that is used to provide BMC COM port functionality.



SPx_DCD	2	1	SPx_DSR
SPx_RXD	4	3	SPx_RTS
SPx_TXD	6	5	SPx_CTS
SPx_DTR	8	7	SPx_RI
GND	10		NC

BMC I2C header (JBMC_I2C1)

This is a 1x4-pin header that is used to provide BMC I2C10 functionality.



1	BMC_I2C_10_SCL
2	BMC_I2C_10_SDA
3	BP_BMC_I2C10_ALERT_N
4	GND

BMC Disable Jumper (JBMC_RST1)

JBMC_RST1	Setting
Short	Reset BMC
Open	Normal (Default)

CMOS Jumper (JCMOS1)

JCMOS1	Setting
Pin1-2	Normal (Default)
Pin2-3	Clear CMOS

BMC Disable Jumper (JBMC_DIS1)

JBMC_DIS1	Setting
Short	Disable BMC ARM boot
Open	Normal (Default)

BMC Reset Password Jumper (JBMC_DEFAULT1)

JBMC_DEFAULT1	Setting
Short	Reset BMC Password
Open	Normal (Default)

CPU SPI Flash Jumper (JBIOS_MUX1、JBIOS_MUX2)

JBIOS_MUX1	JBIOS_MUX2	Setting
Pin1-2	Pin1-2	CPU to Flash Bypass (Default)
Pin1-2	Pin2-3	CPU to PFR Module
Pin2-3	Pin1-2	BMC to Flash Bypass
Pin2-3	Pin2-3	BMC to PFR Module

BMC Socflash Configurations Jumper (JSOC_FLASH1)

JSOC_FLASH1	Setting
Short	Enable
Open	Disable (Default)

BMC SPI MUX Jumper (JBMC_MUX1)

JBMC_MUX1	Setting
Pin1-2	BMC to PFR Module
Pin2-3	BMC to Flash Bypass (Default)

PMBUS Power select Jumper (JPMBUS_SEL1)

JPMBUS_SEL1	Setting
Pin1-2	P3V3_AUX (Default)
Pin2-3	P5V_AUX

NCSI Configurations select Jumper (JNCSI_SEL1)

JNCSI_SEL1	Setting
Pin1-2	LAN (Default)
Pin2-3	I210

3.7 LED

3.7.1 Rear Chassis LEDs

The NIC port/LED should be connected to Vaux (standby) voltage in order to provide the same functionality as stand-up NIC cards for WOL support.

Item		Color	Behavior
NIC 1 – JLAN1	Right	Green (Blinking)	Activity detected.
		Off	LAN cable no connect.
	Left	Status LED	10G : Green, 1G : Yellow, No connect : Off
NIC 2 – JLAN2	Right	Green (Blinking)	Activity detected.
		Off	LAN cable no connect.
	Left	Status LED	10G : Green, 1G : Yellow, No connect : Off
PHY 1 – JRJ45_0	Right	Green (Blinking)	PHY1 activity detected.
		Off	PHY1 is not active, LAN cable no connect.
	Left	Status LED	1G : Orange, 100M : Green, 10M/No connect : Off

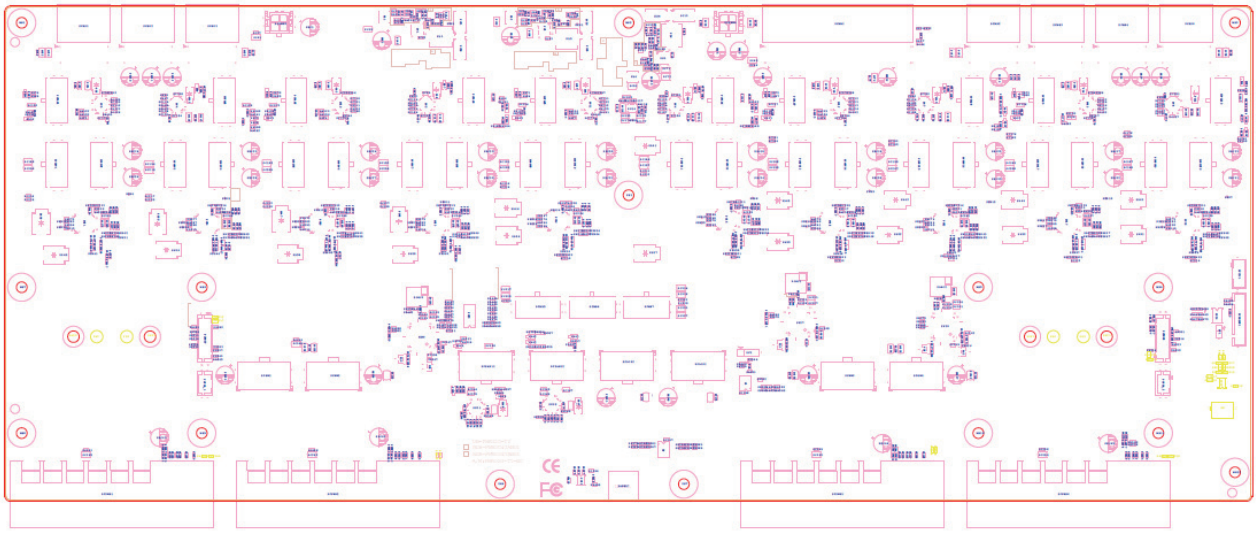
3.7.2 Internal LEDs

Item	Color	Behavior
BMC HEART BEAT LED	Green (Blinking)	BMC activity detected 1. 80Hz : Secure boot failed.(LED 50% on). 2. 20Hz : Boot passed with ABR(Show aout 3s and then exit). 3. 4Hz : ARM CA7 is reading flash or SRAM. 4. 1Hz : ARM CA7 is reading peripherals. 5. 0.5Hz : ARM CA7 is reading DRAM. 6. 0.2Hz : No ARM CA7 read access cycles. 7. 0.1Hz : No ARM CA7 read access cycles over 6~8s. Stay in mode 8 if there is no. ARM CA7 reading access. Exit to mode 4-6 if there is any ARM CA7 reading access.
	Green	BMC is not active.
CPLD DEBUG LED[0:7]	Green/OFF	Refer to CPLD LED mapping table.
CPLD_LED_MODE	Yellow/OFF	Yellow：Port80 MODE, OFF：Sequence MODE.
I210	Green (Blinking)	Activity detected.
	OFF	LAN cable no connect.
	Status LED	1G : Yellow, 100M : Green, No connect : Off
JNGFF1 ACTIVITY LED	Blue (Blinking)	JNGFF1 activity detected.
	OFF	JNGFF1 is not active.
JNGFF2 ACTIVITY LED	Blue (Blinking)	JNGFF2 activity detected.
	OFF	JNGFF2 is not active.

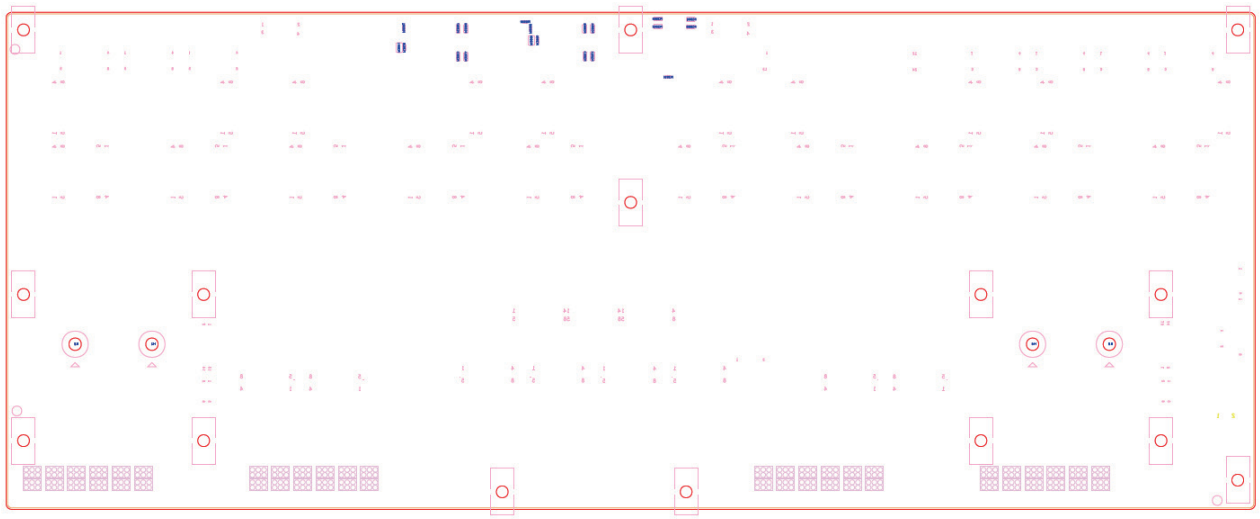
3.8 Power board

3.8.1 Placement

Top view



Bottom view

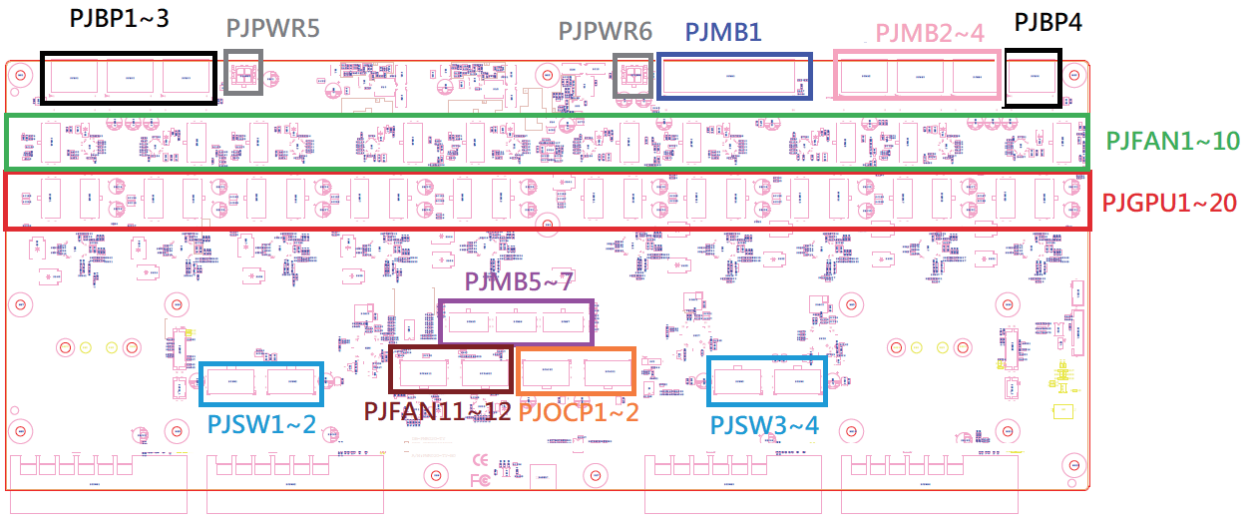


3.8.2 Connector

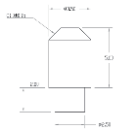
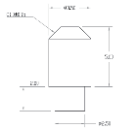
External Connectors

Connector	Description	Function
GPU PWR(PJGPU1~20)	CONN,PWR,C22930-1084N-L_HIGH CURRENT,DIP,P3.0,8P,BLK	FOR GPU POWER 12V/50A/2PCS
FAN PWR(PJFAN1~10)	CONN,PWR,C22930-1084N-L_HIGH CURRENT,DIP,P3.0,8P,BLK	FOR FAN POWER 12V/10A/1PCS
FAN PWR(PJFAN11~12)	CONN,PWR,W4202V-2X04-46GDT,DIP, P4.2,8P,NATURAL	FOR FAN POWER 12V/10A/1PCS
SW BOAED PWR(PJSW1~4)	CONN,PWR,W4202V-2X04-46GDT,DIP, P4.2,8P,NATURAL	FOR SW BOARD POWER
OCP BOAED PWR(PJOCP1~2)	CONN,PWR,W4202V-2X04-46GDT,DIP, P4.2,8P,NATURAL	FOR OCP BOARD POWER
BP PWR(PJBP1~3)	CONN,PWR,W4202V-2X04-46GDT,DIP, P4.2,8P,NATURAL	FOR BP POWER
MB PWR(PJMB1)	CONN,PWR,PWR2X12P-R,DIP,P4.2, 12PX2,TRANSPARENT	FOR MB POWER
MB PWR(PJMB2~4)	CONN,PWR,W4202V-2X04-46GDT, DIP,P4.2,8P,NATURAL	FOR MB POWER
MB PWR(PJMB5~7)	CONN,PWR,C22930-1084N-L_HIGH CURRENT,DIP,P3.0,8P,BLK	FOR MB POWER
Reserved (PJPWR5~6)	CONN,PWR,HIGH CURRENT_MICRO-FIT_2x2P,DIP,P3.0,2X2P,BLK	Reserved

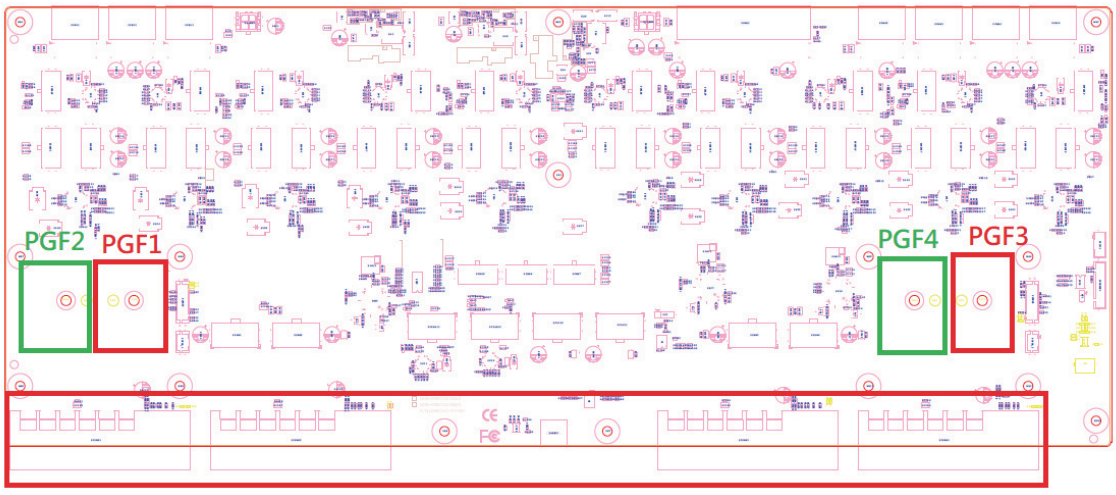
Placement



nternal Connectors

Connector	Description	Function
FROM CRPS(PJPWR1~ PJPWR4)	CONN,PWR,CRPS/RA	CRPS*4
FROM DB-PWR024-TY +12V(PGF1、PGF3)	BUSBAR Nut updated with chamfer. 	+12V
FROM DB-PWR024-TY GND(PGF2、PGF4)	BUSBAR Nut updated with chamfer. 	GND

Placement



PJPWR 1~4

3.8.3 Pin Headers

Connector	Description	Function
PJPWR7	2X7P_VT_D3.6	For DB-PWR024 CRPS signal s used
PJPWR8	2X7P_VT_D3.6	For DB-PWR024 CRPS signals used
PJPDB_1	W2005V-2X03P_VT	For DB-PWR024 CRPS +12V_SB used
PJPDB_2	W2005V-2X03P_VT	For DB-PWR024 CRPS +12V_SB used
PJPMBUS1	JST_1X8P	For I2C4 / I2C6 / PMBUS_ALERT_N / PSU_ON_N / ATX_PW_OK
PJI2C1	JST-2.0MM For	For I2C9

Power Connector (PJPWR7)

VIN_GOOD5_N	1	2	PW5_OK
PRESENT5_N	3	4	SENSE+5
12LS	5	6	SENSE-5
CR_BUS	7	8	ALERT5
GND	9	10	PS5_ON
PMBUS5_A1	11	12	PMBUS2_SCL
PMBUS5_A0	13	14	PMBUS2_SDA

Power Connector (PJPWR8)

VIN_GOOD6 _N	1	2	PW6 _OK
PRESENT6 _N	3	4	SENSE+6
12LS	5	6	SENSE-6
CR_BUS	7	8	ALERT6
GND	9	10	PS6 _ON
PMBUS6 _A1	11	12	PMBUS2_SCL
PMBUS6 _A 0	13	14	PMBUS2_SDA

Power Connector (PJPDB_1)

+12V_AUX	1	2	GND
+12V_AUX	3	4	GND
+12V_AUX	5	6	GND

Power Connector (PJPDB_2)

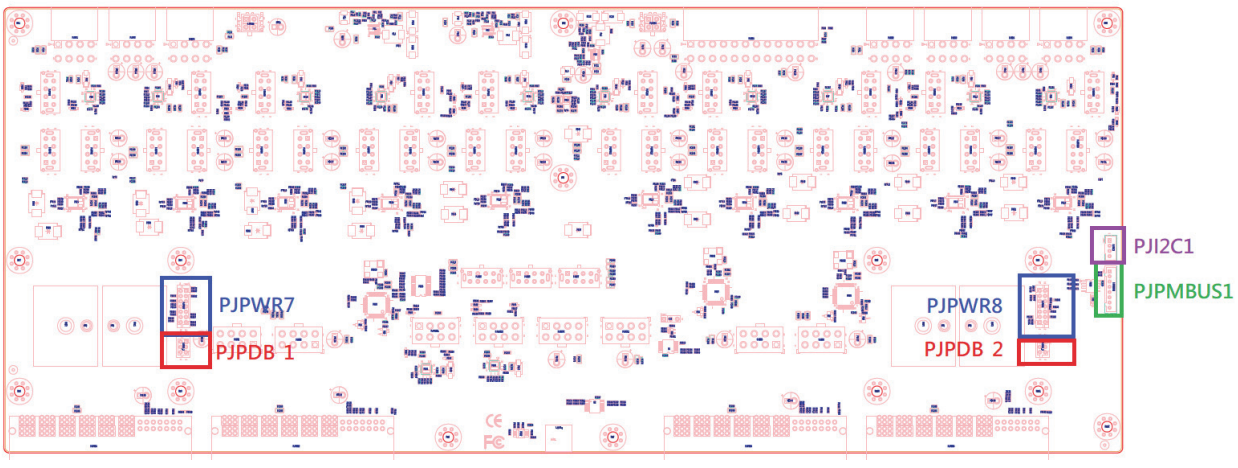
+12V_AUX	1	2	GND
+12V_AUX	3	4	GND
+12V_AUX	5	14	GND

Power Connector (PJPMBUS1)

1	I2C4SCL
2	I2C4SDA
3	PMBUS_ALERT_N
4	I2C6SCL
5	I2C6SDA
6	GND
7	PSU_ON_N
8	ATX_PW_OK

Power Connector (PJI2C1)

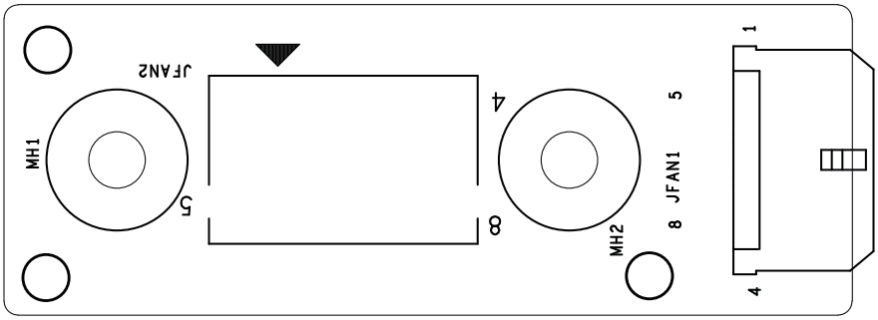
1	I2C9SDA
2	GND
3	I2C9SCL
4	NC



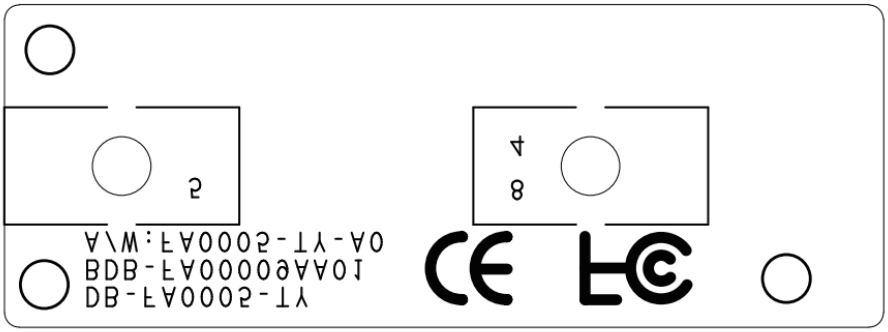
3.9 Fan board

3.9.1 Placement

Top view



Bottom view



3.9.2 Connector

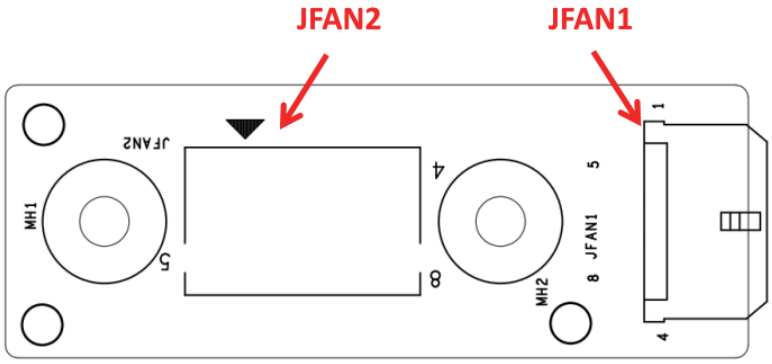
External Connectors

Connector	Description	Function
Fan (JFAN2)	Fan Connector	Fan Connector (+12V, GND, TACH, PWM)

Internal Connectors

Connector	Description	Function
Fan (JFAN1)	Fan Connector	Fan Connector (+12V, GND, TACH, PWM)

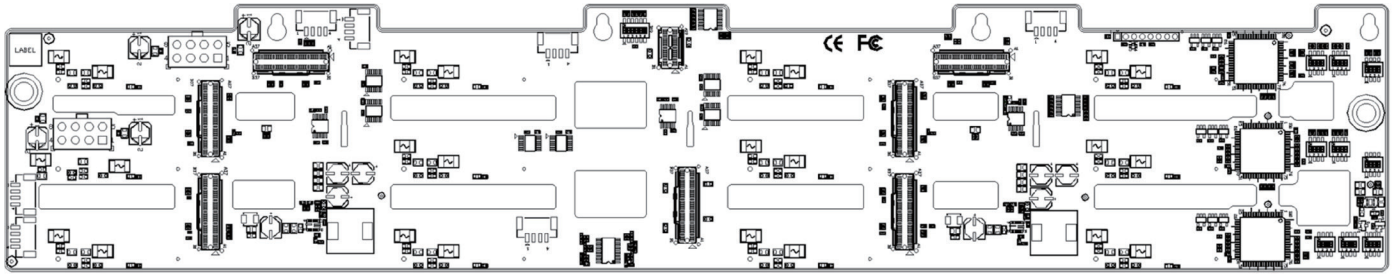
Placement



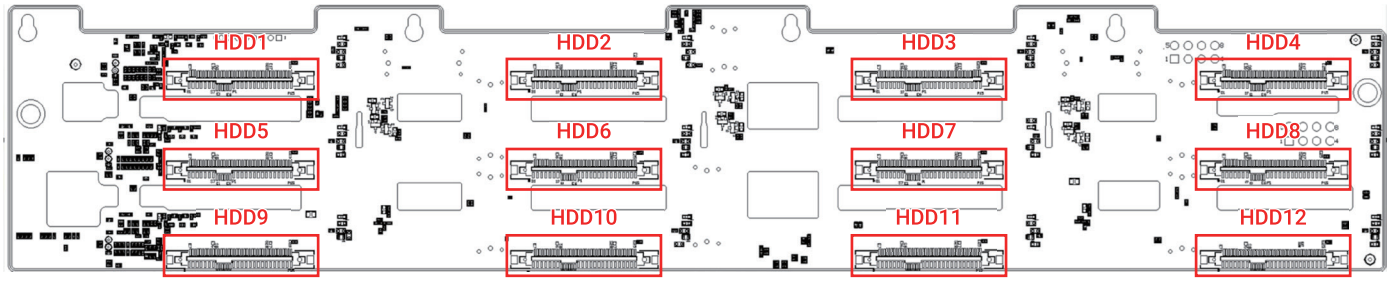
3.10 Backplane: 12 Bay

3.10.1 Placement

Top view



Bottom view



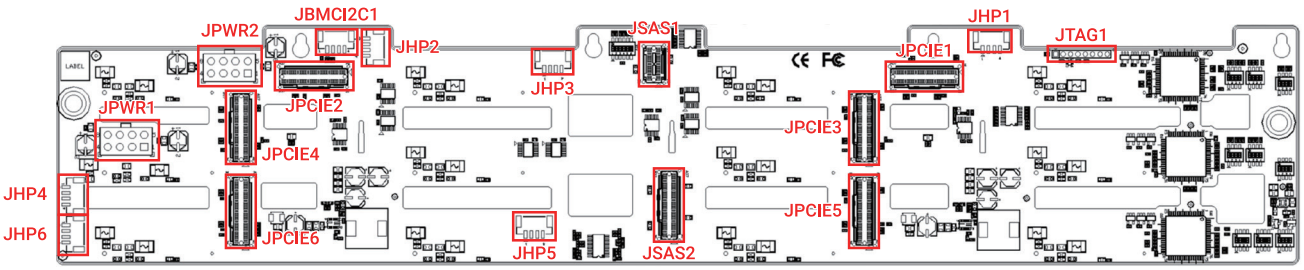
3.10.2 Connector

External Connectors

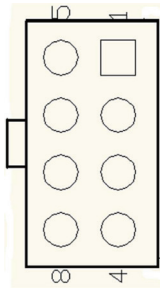
Connector	Description	Function
HDD1~12	SFF-8639 SAS /PCIE Receptacle	HDD connector(Support SAS12G and PCIe Gen4.0)

Internal Connectors

Connector	Description	Function
Power Supply (JPWR1 , JPWR2)	2 x 4 Pin Power Connector	12V 8 A per pin.
Slimline 8i (JPCIE1~ JPCIE6)	74 pin Vertical SFF-8654	PCIE Host connection.
Slimline 8i (JSAS2)	74 pin Vertical SFF-8654	SAS Host connection.
Slimline 4i (JSAS1)	38 pin Vertical SFF-8654	SAS Host connection.
I2C(JBMCI2C1)	4 pin Box-HDR SMT (Pitch 2.0)	I2C Host connection(Control CPLD and I2C Devices ICs Function)
I2C(JHP1~JHP6)	4 pin Box-HDR SMT (Pitch 2.0)	I2C Host connection(Control CPLD Function)
CPLD Header (JTAG1)	1 x 8 Pin Header(Pitch 2.54)	Update CPLD Firmware Header

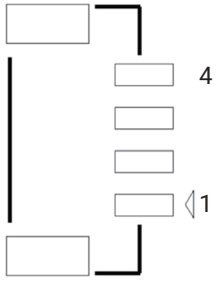


Power Connector (JPWR1,JPWR2)



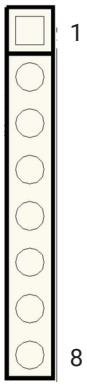
+12V	5	1	GND
+12V	6	2	GND
+12V	7	3	GND
+12V	8	4	GND

I2C Connector (JBMCI2C1)



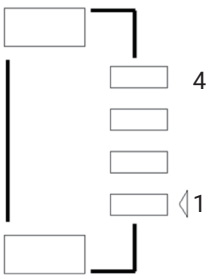
1	SDA
2	GND
3	SCL
4	ALERT_N

CPLD Header (JTAG1)



1	+3V3
2	TDO
3	TDI
4	PROGRAM_L
5	INTI_L
6	TMS
7	GND
8	TCK

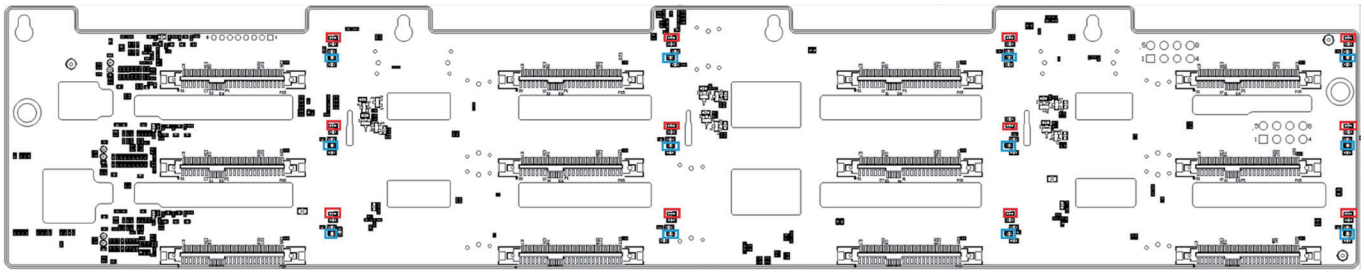
I2C Connector (JHP1~JHP6)



1	SDA
2	GND
3	SCL
4	BP_SHPINT_OUT_N

3.10.3 LEDs

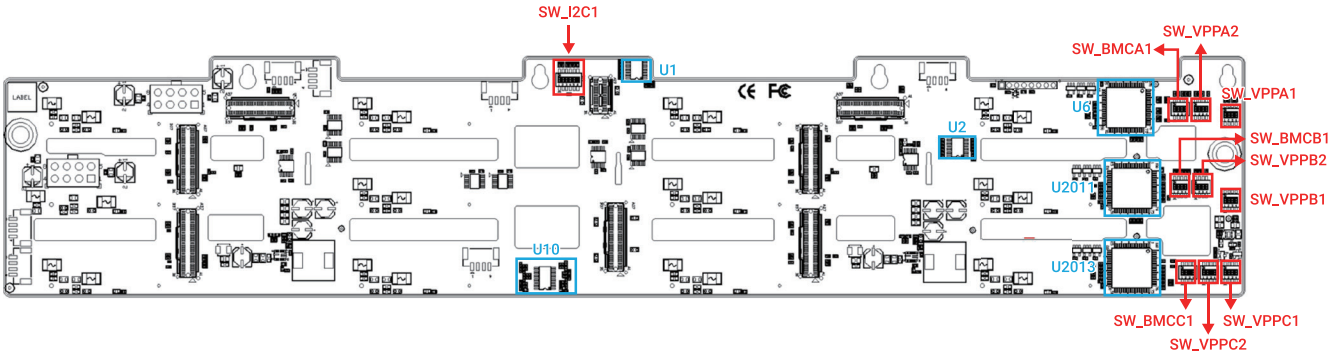
Indicator	Color	Description
HDD Activity LEDs	Blue (On)	HDD present
	Blue (Blinking)	HDD Activity detected
	Off	HDD no connect or Power Off
HDD Locate LEDs	Green	HDD Locate (for NVME HDD)
	Off	NA
HDD Fault/ Status LEDs	Off	Normal
	Yellow (Blinking)	Re-build status/ HDD Locate LEDs (for SAS HDD)
	Yellow (On)	HDD Fault



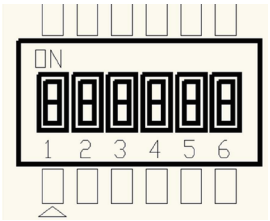
Act
Locate/Fail

3.10.4 Switchs

Placement

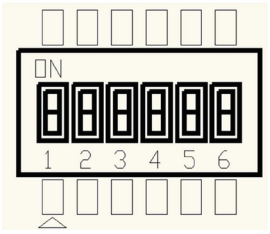


Switchs : (Set U1,U2,U10,U6,U2011,U2013 I2Cs Address)
Switch (SW_I2C1 [U1 I2C Address Define :1110 000X])



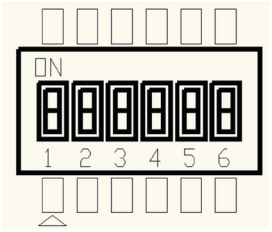
Pin2	Pin1	Address Value
ON	ON	1110 0000 (E0)
ON	OFF	1110 0010 (E2)
OFF	ON	1110 0100 (E4)
OFF	OFF	1110 0110 (E6)

Switch (SW_I2C1 [U10 I2C Address Define :1110 000X])



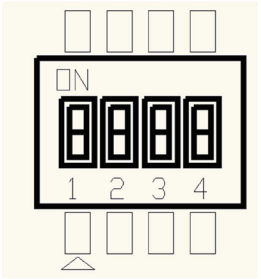
Pin5	Pin4	Pin3	Address Value
ON	ON	ON	1110 0000 (E0)
ON	ON	OFF	1110 0010 (E2)
ON	OFF	ON	1110 0100 (E4)
ON	OFF	OFF	1110 0110 (E6)
OFF	ON	ON	1110 1000 (E8)
OFF	ON	OFF	1110 1010 (EA)
OFF	OFF	ON	1110 1100 (EC)
OFF	OFF	OFF	1110 1110 (EE)

Switch (SW_I2C1 [U2 I2C Address Define : 1110 000X])



Pin4	Pin6	Address Value
ON	ON	1110 0000 (E0)
ON	OFF	1110 0010 (E2)
OFF	ON	1110 0100 (E4)
OFF	OFF	1110 0110 (E6)

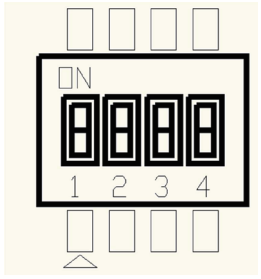
Switch (SW_BMCA1 [U6 I2C Address Define:0110 000X])



Pin3	Pin2	Pin1	Address Value
ON	ON	ON	0110 0000 (60)
ON	ON	OFF	0110 0010 (62)
ON	OFF	ON	0110 0100 (64)
ON	OFF	OFF	0110 0110 (66)
OFF	ON	ON	0110 1000 (68)
OFF	ON	OFF	0110 1010 (6A)
OFF	OFF	ON	0110 1100 (6C)
OFF	OFF	OFF	0110 1110 (6E)

*Pin4 OFF-> Disable VPP & BMC I2C Output (Disable the VPP & BMC I2C Output of JPCIE1 & JPCIE2)
Pin4 ON-> Enable VPP & BMC I2C Output(Enable the VPP & BMC I2C Output of JPCIE1 & JPCIE2)

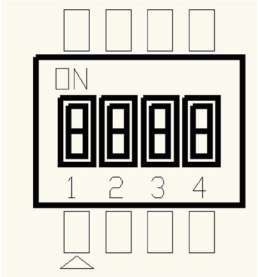
Switch (SW_VPPA1 [U6 I2C Address Define:0100 000X])



Pin3	Pin2	Pin1	Address Value
ON	ON	ON	0100 0000 (40)
ON	ON	OFF	0100 0010 (42)
ON	OFF	ON	0100 0100 (44)
ON	OFF	OFF	0100 0110 (46)
OFF	ON	ON	0100 1000 (48)
OFF	ON	OFF	0100 1010 (4A)
OFF	OFF	ON	0100 1100 (4C)
OFF	OFF	OFF	0100 1110 (4E)

*Pin4 OFF-> Select VPP I2C Output (Set the VPP I2C output of JPCIE1)
Pin4 ON-> Select BMC I2C Output (Set the BMC I2C output of JPCIE1)

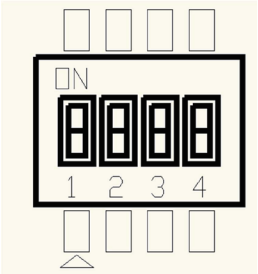
Switch (SW_VPPA2 [U6 I2C Address Define:0100 000X])



Pin3	Pin2	Pin1	Address Value
ON	ON	ON	0100 0000 (40)
ON	ON	OFF	0100 0010 (42)
ON	OFF	ON	0100 0100 (44)
ON	OFF	OFF	0100 0110 (46)
OFF	ON	ON	0100 1000 (48)
OFF	ON	OFF	0100 1010 (4A)
OFF	OFF	ON	0100 1100 (4C)
OFF	OFF	OFF	0100 1110 (4E)

*Pin4 OFF -> Select VPP I2C Output (Set the VPP I2C output of JPCIE2)
Pin4 ON -> Select BMC I2C Output (Set the BMC I2C output of JPCIE2)

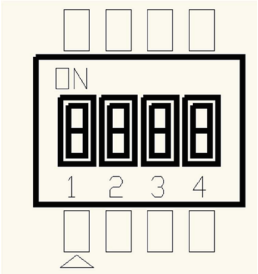
Switch (SW_BMCB1 [U2011 I2C Address Define:0110 000X])



Pin3	Pin2	Pin1	Address Value
ON	ON	ON	0110 0000 (60)
ON	ON	OFF	0110 0010 (62)
ON	OFF	ON	0110 0100 (64)
ON	OFF	OFF	0110 0110 (66)
OFF	ON	ON	0110 1000 (68)
OFF	ON	OFF	0110 1010 (6A)
OFF	OFF	ON	0110 1100 (6C)
OFF	OFF	OFF	0110 1110 (6E)

*Pin4 OFF-> Disable VPP & BMC I2C Output (Disable the VPP & BMC I2C Output of JPCIE3 & JPCIE4)
Pin4 ON-> Enable VPP & BMC I2C Output(Enable the VPP & BMC I2C Output of JPCIE3 & JPCIE4)

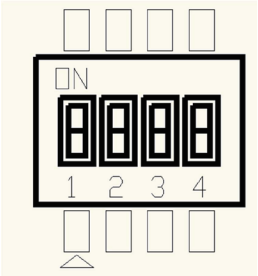
Switch (SW_VPPB1 [U2011 I2C Address Define:0100 000X])



Pin3	Pin2	Pin1	Address Value
ON	ON	ON	0100 0000 (40)
ON	ON	OFF	0100 0010 (42)
ON	OFF	ON	0100 0100 (44)
ON	OFF	OFF	0100 0110 (46)
OFF	ON	ON	0100 1000 (48)
OFF	ON	OFF	0100 1010 (4A)
OFF	OFF	ON	0100 1100 (4C)
OFF	OFF	OFF	0100 1110 (4E)

*Pin4 OFF-> Select VPP I2C Output (Set the VPP I2C output of JPCIE3)
Pin4 ON-> Select BMC I2C Output (Set the BMC I2C output of JPCIE3)

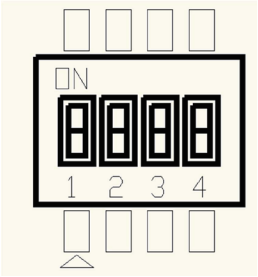
Switch (SW_VPPB2 [U2011 I2C Address Define:0100 000X])



Pin3	Pin2	Pin1	Address Value
ON	ON	ON	0100 0000 (40)
ON	ON	OFF	0100 0010 (42)
ON	OFF	ON	0100 0100 (44)
ON	OFF	OFF	0100 0110 (46)
OFF	ON	ON	0100 1000 (48)
OFF	ON	OFF	0100 1010 (4A)
OFF	OFF	ON	0100 1100 (4C)
OFF	OFF	OFF	0100 1110 (4E)

*Pin4 OFF-> Select VPP I2C Output (Set the VPP I2C output of JPCIE4)
Pin4 ON-> Select BMC I2C Output (Set the BMC I2C output of JPCIE4)

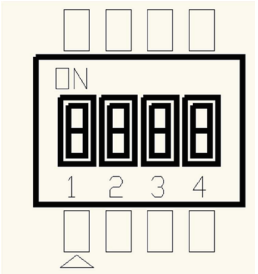
Switch (SW_BMCC1 [U2013 I2C Address Define:0110 000X])



Pin3	Pin2	Pin1	Address Value
ON	ON	ON	0110 0000 (60)
ON	ON	OFF	0110 0010 (62)
ON	OFF	ON	0110 0100 (64)
ON	OFF	OFF	0110 0110 (66)
OFF	ON	ON	0110 1000 (68)
OFF	ON	OFF	0110 1010 (6A)
OFF	OFF	ON	0110 1100 (6C)
OFF	OFF	OFF	0110 1110 (6E)

*Pin4 OFF-> Disable VPP & BMC I2C Output (Disable the VPP & BMC I2C Output of JPCIE5 & JPCIE6)
Pin4 ON-> Enable VPP & BMC I2C Output(Enable the VPP & BMC I2C Output of JPCIE5 & JPCIE6)

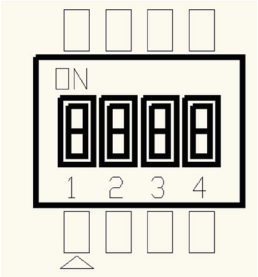
Switch (SW_VPPC1 [U2013 I2C Address Define:0100 000X])



Pin3	Pin2	Pin1	Address Value
ON	ON	ON	0100 0000 (40)
ON	ON	OFF	0100 0010 (42)
ON	OFF	ON	0100 0100 (44)
ON	OFF	OFF	0100 0110 (46)
OFF	ON	ON	0100 1000 (48)
OFF	ON	OFF	0100 1010 (4A)
OFF	OFF	ON	0100 1100 (4C)
OFF	OFF	OFF	0100 1110 (4E)

*Pin4 OFF-> Select VPP I2C Output (Set the VPP I2C output of JPCIE5)
Pin4 ON-> Select BMC I2C Output (Set the BMC I2C output of JPCIE5)

Switch (SW_VPPC2 [U2013 I2C Address Define:0100 000X])



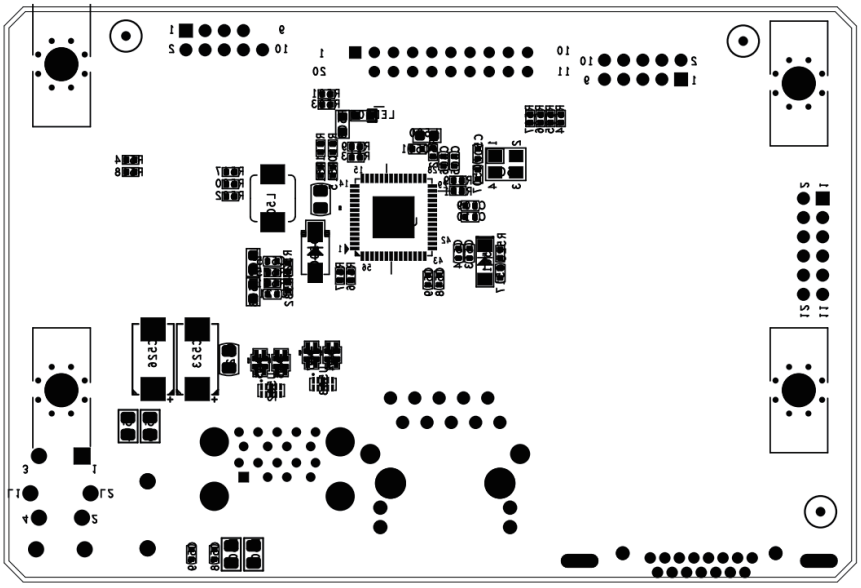
Pin3	Pin2	Pin1	Address Value
ON	ON	ON	0100 0000 (40)
ON	ON	OFF	0100 0010 (42)
ON	OFF	ON	0100 0100 (44)
ON	OFF	OFF	0100 0110 (46)
OFF	ON	ON	0100 1000 (48)
OFF	ON	OFF	0100 1010 (4A)
OFF	OFF	ON	0100 1100 (4C)
OFF	OFF	OFF	0100 1110 (4E)

*Pin4 OFF-> Select VPP I2C Output (Set the VPP I2C output of JPCIE6)
Pin4 ON-> Select BMC I2C Output (Set the BMC I2C output of JPCIE6)

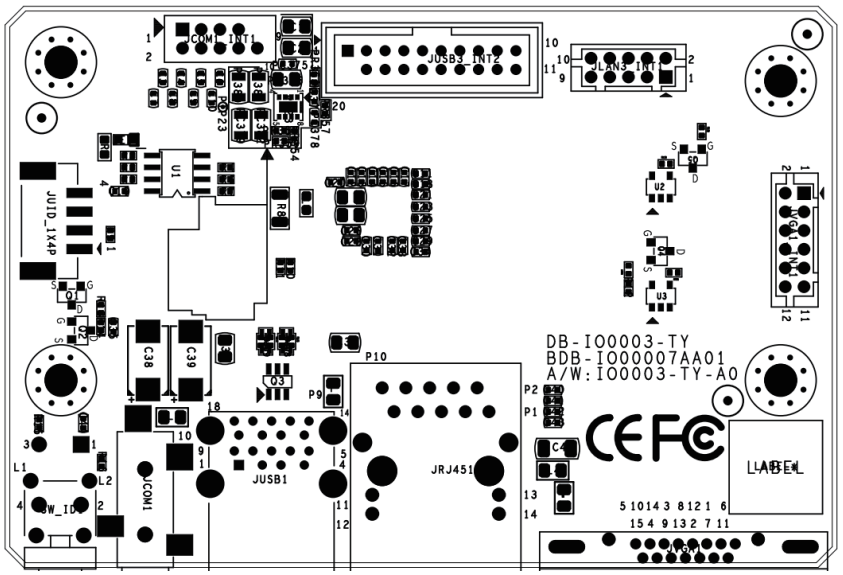
3.11 IO board

3.11.1 Placement

Bottom side



Top side



3.11.2 Connector

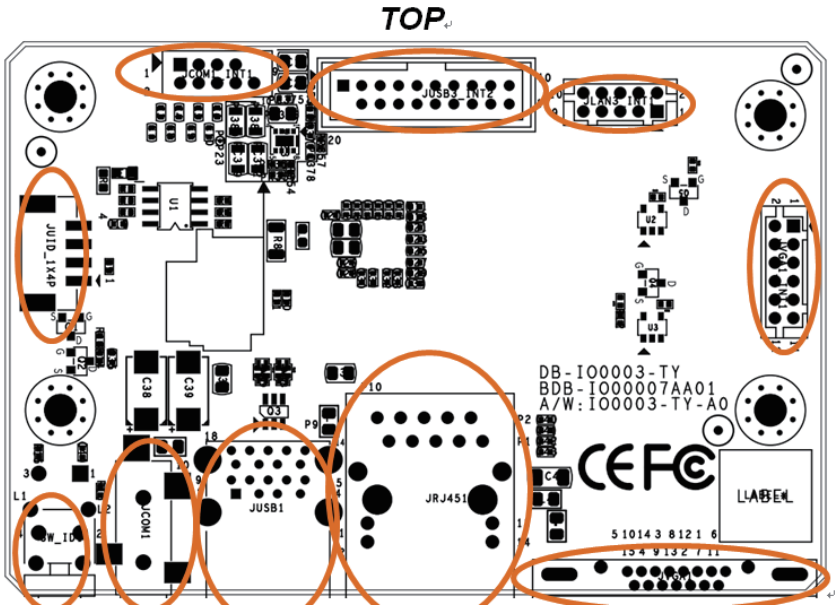
External Connectors

Connector	Description	Function
JUSB1	External USB3.0 Conn	External USB3.0 Conn
JRJ451	External 1G RJ45 Conn	External 1G RJ45 Conn
JCOM1	External Phone jack	External Phone jack
UID LED BUTTON(SW_ID1)	UID Button	UID Button (BLU)
JVGA1	External VGA Conn	External VGA Conn

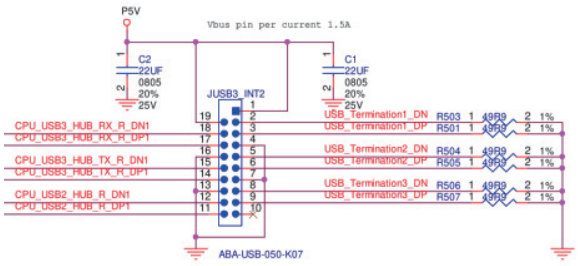
Internal Connectors

Connector	Description	Function
19P Internal USB3.0 Conn(JUSB3_INT2)	Internal USB3.0 conn	USB3.0
Internal Lan conn(JLAN3_INT1)	Internal I210 1g LAN conn	Internal I210 1g LAN conn
Internal COM Header(JCOM1_INT1)	Internal COM Header	Internal COM Header
UID LED Button Header(JUID_1X4P)	Internal UID Header	Internal UID Header
Internal VGA Conn (JVGA_INT1)	Internal VGA Conn	Internal VGA Conn

Placement

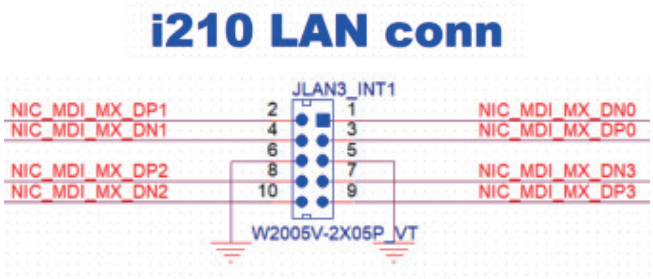


19P Internal USB3.0 (JUSB3_INT2)



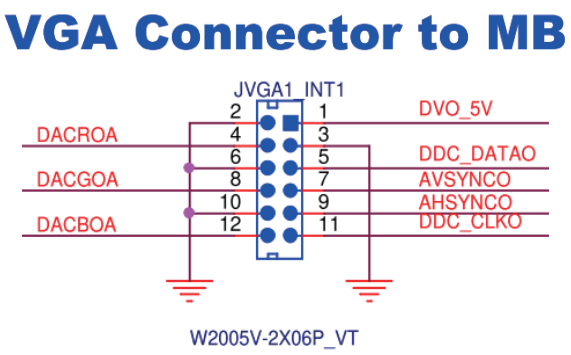
P5V	1	11	CPU_USB2_HUB_R_DP1
USB_Termination1_DN	2	12	CPU_USB2_HUB_R_DN1
USB_Termination1_DP	3	13	GND
GND	4	14	CPU_USB3_HUB_TX_R_DP1
USB_Termination2_DN	5	15	CPU_USB3_HUB_TX_R_DN1
USB_Termination2_DP	6	16	GND
GND	7	17	CPU_USB3_HUB_RX_R_DP1
USB_Termination3_DN	8	18	CPU_USB3_HUB_RX_R_DN1
USB_Termination3_DP	9	19	P5V
NC	10		

Internal Lan conn (JLAN3_INT1)



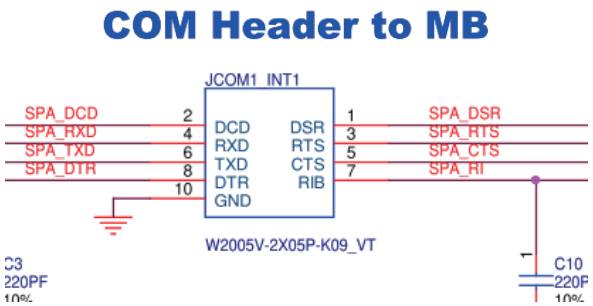
NIC_MDI_MX_DN0	1	2	NIC_MDI_MX_DP1
NIC_MDI_MX_DP0	3	4	NIC_MDI_MX_DN1
GND	5	6	GND
NIC_MDI_MX_DN3	7	8	NIC_MDI_MX_DP2
NIC_MDI_MX_DP3	9	10	NIC_MDI_MX_DN2

Internal VGA conn (JVGA1_INT1)



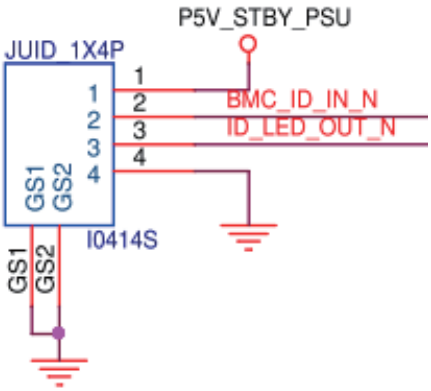
DVO_5V	1	2	GND
GND	3	4	DACROA
DDC_DATAO	5	6	GND
AVSYNCO	7	8	DACGOA
AHSYNCO	9	10	GND
DDC_CLKO	11	12	DACBOA

Internal com header (JCOM1_INT1)



SPA_DSR	1	2	SPA_DCD
SPA_RTS	3	4	SPA_RXD
SPA_CTS	5	6	SPA_TXD
SPA_RI	7	8	SPA_DTR
		10	GND

UID header (JUID_1X4P)



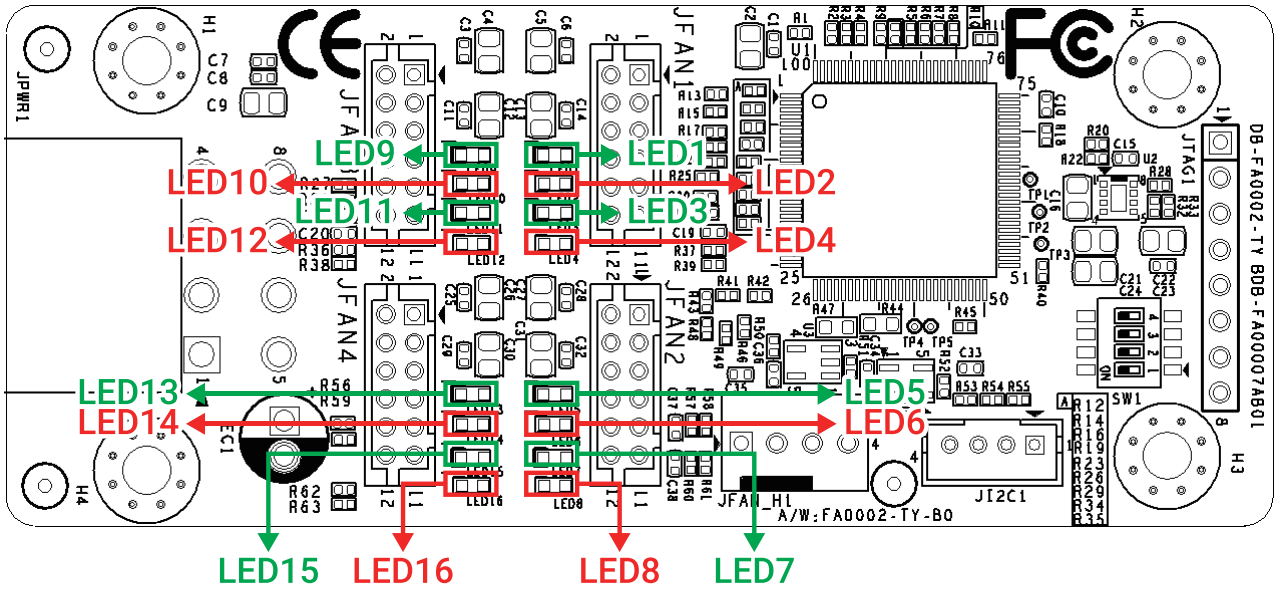
1	P5V_STBY_PSU
2	BMC_ID_IN_N
3	ID_LED_OUT_N
4	GND

3.11.3 LED Button Definition

Item	Color	Behavior
UID Button LED BLU (SW1)	Blue (on)=UID Enabled	On/off can be controlled by BMC
	Blue(off)=UID Disabled	On/off can be controlled by BMC

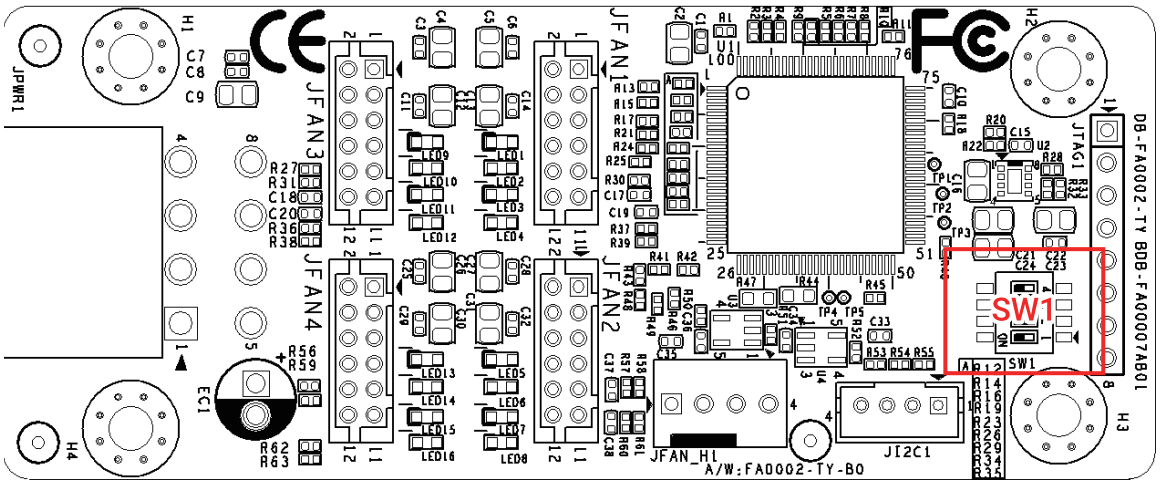
3.11.3 LEDs

Indicator	Color	Description		Indicator	Color	Description	
LED1	Green	Light	FAN1 SCAN	LED9	Green	Light	FAN5 SCAN
		Off	NA			Off	NA
LED2	Red	Light	FAN1 Fault	LED10	Red	Light	FAN5 Fault
		Off	NA			Off	NA
LED3	Green	Light	FAN2 SCAN	LED11	Green	Light	FAN6 SCAN
		Off	NA			Off	NA
LED4	Red	Light	FAN2 Fault	LED12	Red	Light	FAN6 Fault
		Off	NA			Off	NA
LED5	Green	Light	FAN3 SCAN	LED13	Green	Light	FAN3 SCAN
		Off	NA			Off	NA
LED6	Red	Light	FAN3 Fault	LED14	Red	Light	FAN7 Fault
		Off	NA			Off	NA
LED7	Green	Light	FAN4 SCAN	LED15	Green	Light	FAN4 SCAN
		Off	NA			Off	NA
LED8	Red	Light	FAN4 Fault	LED16	Red	Light	FAN4 Fault
		Off	NA			Off	NA



3.11.4 DIP Switch

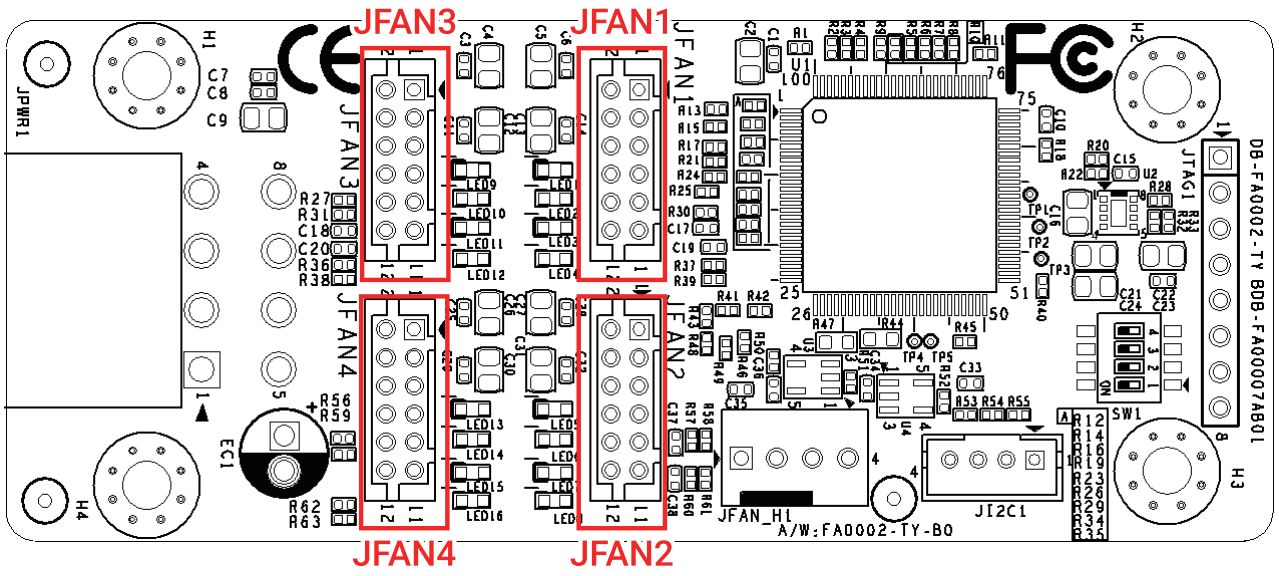
Top view



Switch (SW1)

Pin3	Pin2	Pin1	Fan NUMBER	Pin4	Mode Sel
OFF	OFF	OFF	1	OFF	latch
OFF	OFF	ON	2	ON	polling(default)
OFF	ON	OFF	3		
OFF	ON	ON	4		
ON	OFF	OFF	5		
ON	OFF	ON	6		
ON	ON	OFF	7		
ON	ON	ON	8(default)		

3.11.5 Fan Mapping



Location	Function
JFAN1	FAN1
	FAN2
JFAN2	FAN3
	FAN4
JFAN3	FAN5
	FAN6
JFAN4	FAN7
	FAN8

Chapter 4. BIOS Configuration Settings

This chapter demonstrates how to configure the UEFI BIOS settings in your system device. You can enter the BIOS screen during system startup.

To enter BIOS configuration settings,
- Press **Esc** key during the Power-On-Self-Test (POST)

To enter BIOS after POST, you have to restart the system by using one of the three methods:
- Press **Ctrl** + **Alt** + **Delete.**
- Press the reset button on the system chassis.
- Turn the system off and on.

NOTE
- The following pages provide the details of BIOS menu. Please be noted that the BIOS menu are continually changing due to the BIOS updating. The BIOS menu provided are the most updated ones when this manual is written.
- The default value for each BIOS option key may vary per system. The [default] key is for reference only.

4.1 Navigation Keys

The navigation keys are listed below.

Function Key	Description
< ↑ > < ← > < → > < ↓ >	Select item.
< Enter >	Select and enter sub-screen.
< + > < - >	Modify selected option.
< F1 >	General help.
< F2 >	Previous Value.
< F3 >	Optimized defaults.
< F4 >	Save & Exit.
< Esc >	Exit the current menu screen.

4.2 BIOS Menu

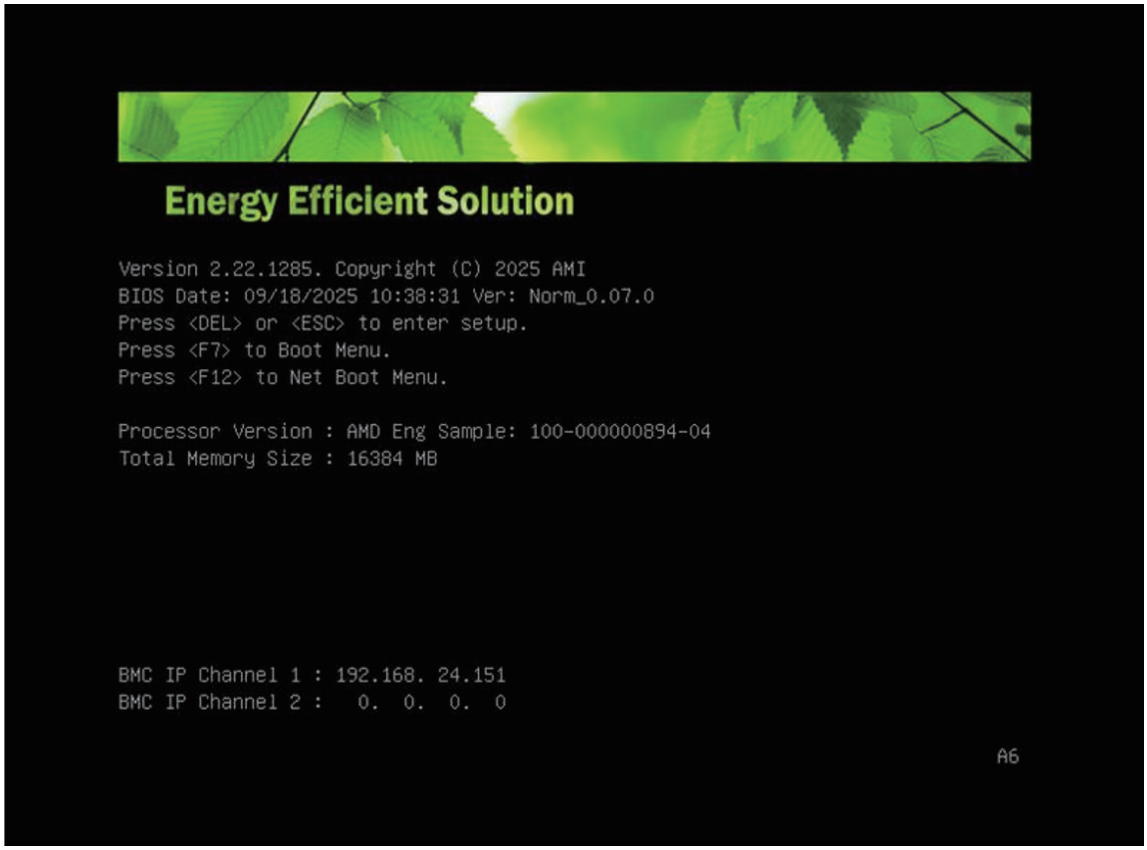
4.2.1 Menu

Press ⬅ and ➡ to select the options of the menu bar.
Press **Enter** to access the option screen.

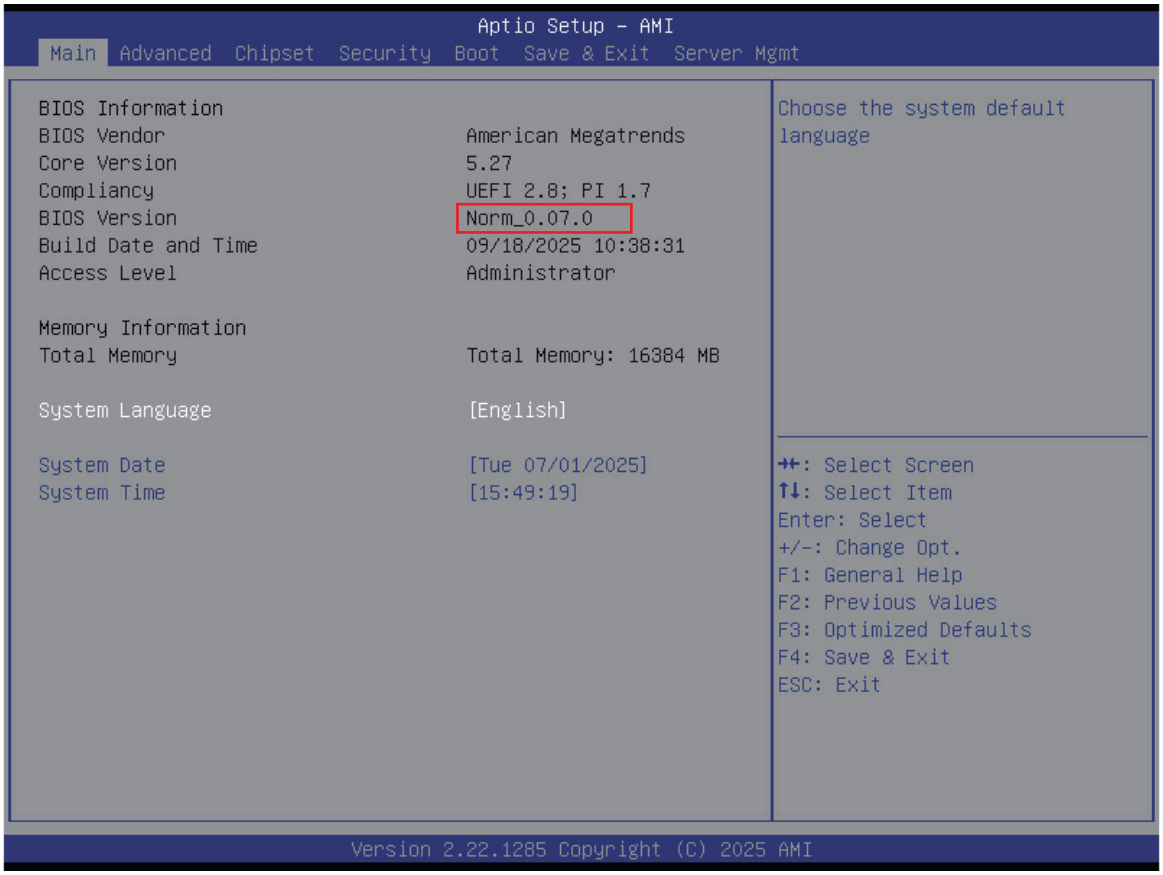
Menu	Description
Main	Displays basic system information and date & time.
Advanced	Allows configuration of advanced system settings.
Platform Configuration	Allows configuration of platform settings such as PCH, miscellaneous, and server ME configuration.
Socket Configuration	Allows configuration of socket settings such as processor, Common RefCode, UPI, and memory configurataion.
Server Management	Allows configuration of timer, System Event Log, and BMC network.
Security	Sets passwords and security functions.
Boot	Sets boot options such as Quick Boot or USB Boot.
Exit	Save changes and exit, discard changes and exit, discard changes, or load optimal or fail-safe defaults.

4.2.2 Startup

① Press **DEL** or **ESC** to run the BIOS setup procedure.



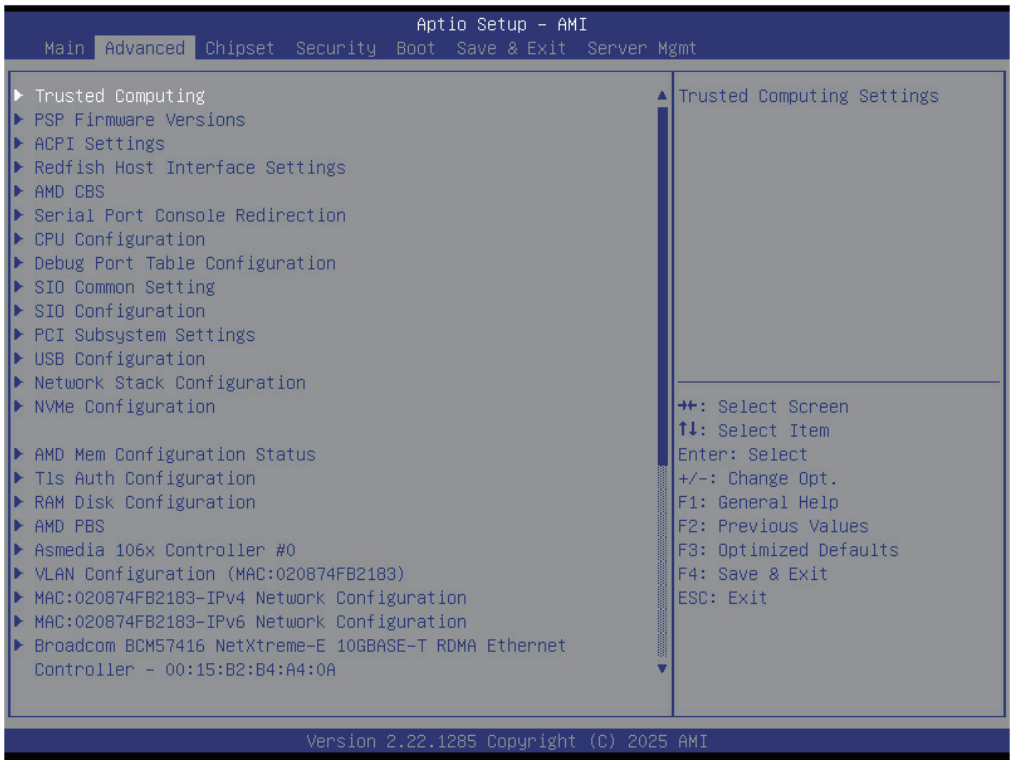
4.3 Main



4.3.1 Main

Main	
System Language	Configures the language used in the system.
System time	Configures the current time.
System date	Configures the current date.

4.4 Advanced



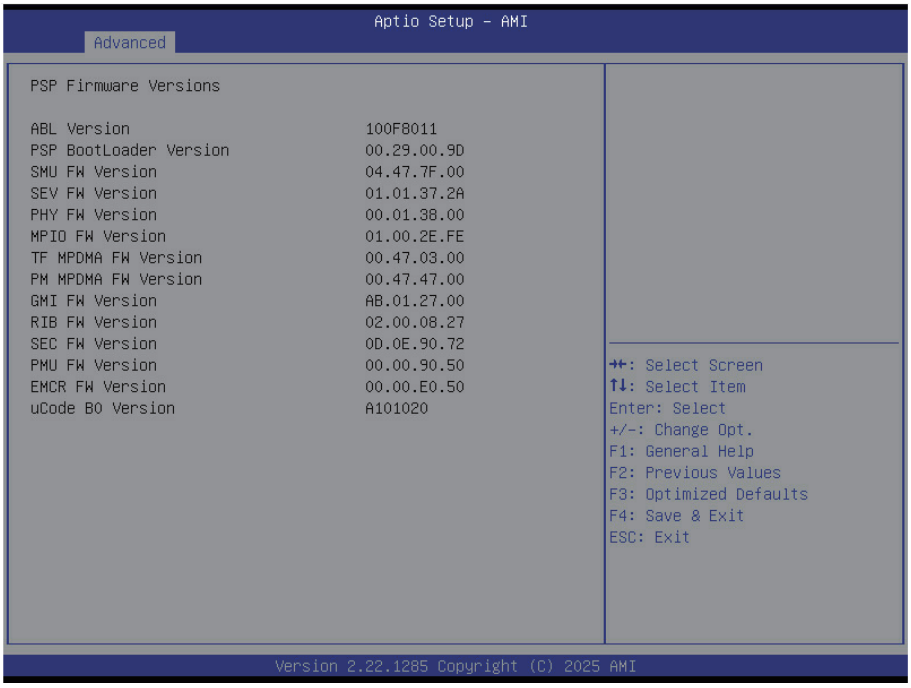
4.4.1 Trusted Computing

Trusted Computing Settings.

Trusted Computing			
Security Device Support	Enables/disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
	▶Enable	Disable	
SHA256 PCR Bank	Enables/disables SHA-256 PCR Bank.		
	▶Enabled	Disabled	
SHA384 PCR Bank	Enables/disables SHA-384 PCR Bank.		
	Enabled	▶Disabled	
Pending opertation	Schedules an operation for the security deivce. NOTE: Your computer will reboot during restart in order to change the state of the security device.		
	▶None	TPM Clear	
Platform Hierarchy	Enables/disables platform hierarchy.		
	▶Enabled	Disabled	
Storage Hierarchy	Enables/disables storage hierarchy.		
	▶Enabled	Disabled	
Endorsement Hierarchy	Enables/disables endorsement hierarchy.		
	▶Enabled	Disabled	
Physical Presence Spec Version	Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3 Note some HCK tests might not support 1.3.		
	1.2	▶1.3	
PH Randomization	Enables/disables Platform Hierarchy randomization. Do not enable this question in production platforms. This is for development testing. Override change Platform AUth ELINK for production platforms supporting TXT.		
	▶Enabled	Disabled	
Device Select	• TPM 1.2: TPM 1.2 will restrict support to TPM 1.2 devices. • TPM 2.0: TPM 2.0 will restrict support to TPM 2.0 devices. • Auto: Auto will support both with the defualt set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.		
	▶Auto	TPM 1.2	TPM 2.0

4.4.2 PSP Firmware Versions

PSP Firmware Versions



4.4.3 ACPI Settings

System ACPI Parameters.

ACPI Settings		
Enable ACPI Auto Configuration	Enables/disables BIOS ACPI Auto Configuration.	
	Enabled	▶Disabled

4.4.4 Redfish Host Interface Settings

Redfish Host Interface Parameters.

Redfish Host Interface Settings			
Redfish	Enables/disables AMI Redfish.		
	▶Enabled	Disabled	
Authentication mode	Select authentication mode.		
	▶Basic Authentication	Session Authentication	Authentication None

4.4.5 AMD CBS

AMD CBS Setup Page.

AMD CBS							
CPU Common Options	Performance	OC Mode	Select overclock operation modes.				
			▶Normal Operation	Customized			
		CCD/Core/ Thread Enablement	CCD Control	Sets the number of active CCDs. Once this option has been used to remove any CCDs, a Power Cycle is required in order for future selections to take effect.			
				▶Auto	2 CCDs	4 CCDs	
				6 CCDs	8 CCDs	10 CCDs	
			Core Control	Sets the number of cores to be used. Once this option has been used to remove any cores, a Power Cycle is required in order for future selections to take effect.			
				▶Auto	ONE (1+0)	TWO (2+0)	THREE (3+0)
				FOUR (4+0)	FIVE (5+0)	SIX (6+0)	SEVEN (7+0)
		SMT Control	Can be used to disable symmetric multithreading. To re-enable SMT, a Power Cycle is needed after selecting the 'Enable' option. Select 'Auto' base on BIOS PCD (PcdAmdSmtMode) default setting. WARNING–S3 is NOT SUPPORTED on systems where SMT is disabled.				
			▶Auto	Enable	Disable		
		Enable Requested CPU min frequency	This allows for minimum requested CPU frequency to be used.				
			Enable	▶Disable			
	REP-MOV/ STOS Streaming	Allow REP-MOVS/STOS to use non-caching streaming stores for large sizes.					
		▶Enabled	Disabled				
	Prefetcher settings	L1 Stream HW Prefetcher	Option to Enable/Disable L1 Stream HW Prefetcher.				
			▶Auto	Enable	Disable		
		L1 Stride Prefetcher	Uses memory access history of individual instructions to fetch additional lines when each access is a constant distance from the previous.				
			▶Auto	Enable	Disable		
		L1 Region Prefetcher	Uses memory access history to fetch additional lines when the data access for a given instruction tends to be followed by other data accesses.				
			▶Auto	Enable	Disable		
		L2 Stream HW Prefetcher	Option to Enable/Disable L2 Stream HW Prefetcher				
			▶Auto	Enable	Disable		
		L2 Up/Down Prefetcher	Uses memory access history to determine whether to fetch the next or previous line for all memory accesses.				
			▶Auto	Enable	Disable		
		L1 Burst Prefetch Mode	Option to Enable/Disable L1 Burst Prefetch Mode.				
			▶Auto	Enable	Disable		
	Core Watchdog	Core Watchdog Timer Enable	Enable/Disable CPU Watchdog Timer.				
			▶Auto	Enabled	Disabled		
	Redirection For Return Dis	From a workaround for GCC/C000005 issue for XV Core on CZ A0, setting MSRC001_1029 Decode Configuration (DE_CFG) bit 14 [DecfgNoRdrctForReturns] to 1					
		▶Auto	1	0			
	Platform First Error Handling	Enable/disable PFEH, clock individual banks, and mask deferred error interrupts from each bank.					
		▶Auto	Enabled	Disabled			
	Core Performance Boost	Disable CPB.					
		▶Auto	Disabled				
	Global C-state Control	Controls I0 based C-state generation and DF C-state.					
		▶Auto	Enabled	Disabled			
	Power Supply Idle Control	Power Supply Idle Control.					
		▶Auto	Low Current Idle	Typical Current Idle			

CPU Common Options	SEV-ES ASID Space Limit	SEV-ES and SNP guests must use ASIDs in the range 1 through(this value-1). SEV guests must use ASIDs in the range of this value through 1007. To have all ASIDs support SEV-ES or SNP guests, set this value to 1007. The default is 1: all SEV guests and no SEV-ES or SNP guests.			
		1			
	SEV Control	Can be used to disable SEV. To re-enable SEV, a Power Cycle is needed after selecting the 'Enable' option.			
		▶Enable	Disable		
	Streaming Stores Control	Enable/disable the streaming stores functionality.			
		▶Auto	Enabled	Disabled	
	Local APIC Mode	Select local APIC operation modes.			
		▶Auto	Compatibility	xAPIC	x2APIC
	ACPI _CST C1 Declaration	Determines whether or not to declare the C1 state to the OS.			
		▶Auto	Enabled	Disabled	
	ACPI CST C2 Latency	Enter in microseconds (decimal value). Larger C2 latency values will reduce the number of C2 transitions and reduce C2 residency. Fewer transitions can help when performance is sensitive to the latency of C2 entry and exit. Higher residency can improve performance by allowing higher frequency boost and reduce idle core power. With Linux kernel 6.0 or later, the C2 transition cost is significantly reduced. The best value will be dependent on kernel version, use case, and workload.			
		800			
	MCA error thresh enable	Enable MCA error thresholding.			
		▶Auto	True	False	
	MCA FruText	Enable MCA FruText.			
		▶True	False		
	SMU and PSP Debug Mode	When this option is enabled, uncorrected errors detected by the PSP FW or SMU FW that should cause a cold reset, will hang and not reset the system.			
		▶Auto	Enabled	Disabled	
	PPIN Opt-in	Turn on PPIN feature			
		▶Auto	Enabled	Disabled	
	SNP Memory (RMP Table) Coverage	Enabled=ENTIRE system memory is covered.			
		▶Auto	Enabled	Disabled	Custom
	SMEE	Control secure memory encryption enable. Enabling both SMEE and SME-MK is not supported. Results in #GP.			
		▶Auto	Enable	Disable	
	Action on BIST Failure	Action to take when a CCD BIST failure is detected.			
		▶Auto	Do noting	Down-CCD	
	Fast Short REP MOVSB (FSRM)	Default is 1, can be set to zero for analysis purposes as long as OS supports it.			
		▶Auto	Enabled	Disabled	
	Enhanced REP MOVSB/ STOSB (ERSM)	Default is 1, can be set to zero for analysis purposes as long as OS supports it.			
		▶Auto	Enabled	Disabled	

CPU Common Options	Log Transparent Errors	Log transparent errors in MCA in addition to debug registers.				
		▶Auto	Enabled	Disabled		
	AVX512	Enable/Disable AVX512.				
		▶Auto	Enabled	Disabled		
	MONITOR and MWAIT disable	The MONITOR, MWAIT, MONITORX, and MWAITX opcodes become invalid, when Enabled.				
		▶Auto	Enabled	Disabled		
	Small Hammer Configuration	Enabled: LS_CFG::DisSpecWcReq= 0 LS_CFG3::DisSpecWcNonStrmLd = 1 LS_CFG3::EnLockNeedProgressForSpecNC = 1 Disabled: LS_CFG::DisSpecWcReq= 0 LS_CFG3::DisSpecWcNonStrmLd = 0 LS_CFG3::EnLockNeedProgressForSpecNC = 0				
		▶Auto	Enabled	Disabled		
	Corrector Branch Predictor	Enabling for branch heavy codes may reduce conditional branch mispredicts				
		▶Disable	Enable			
	PAUSE Delay	Number a cycles thread will be idle after a PAUSE instruction.				
		▶Auto	Disable	16 cycles	32 cycles	64 cycles	128 cycles
	CPU Speculative Store Modes	Balanced: Store instructions may delay sending out their invalidations to remote cacheline copies when the cacheline is present but not in a writable state in the local cache. More Speculative: Store instructions will send out invalidations to remote cacheline copies as soon as possible. Less Speculative: Store instructions may delay sending out their invalidations to remote cacheline copies when the cacheline is not present in the local cache or not in a writable state in the local cache.				
		▶Auto	Balanced	More Speculative	Less Speculative	
	Prefetch/ Request Throttle	Enables XI logic which calculates average latency, updates throttle level, and sends throttle level messages to L2				
		▶Auto	Enable	Disable		
DF Common Options	Memory Addressing	NUMA nodes per socket	Specifies the number of desired NUMA nodes per socket. Zero will attempt to interleave the two sockets together.			
			▶Auto	NPS0	NPS1	NPS2	NPS4
		Memory interleaving	Allows for disabling memory interleaving. Note that NUMA nodes per socket will be honored regardless of this setting.			
			▶Auto	Enabled	Disabled	
		1TB remap	Attempt to remap DRAM out of the space just below the 1TB boundary. The ability to remap depends on DRAM configuration, NPS, and interleaving selection, and may not always be possible.			
			▶Auto	Do not remap	Attempt to remap	
		DRAM map inversion	Inverting the map will cause the highest memory channels to get assigned the lowest addresses in the system.			
			▶Auto	Enabled	Disabled	
		Location of private memory regions	Controls whether or not the private memory regions (PSP, SMU and CC6) are at the top of DRAM, at the top of 1st DRAM pair or distributed. Note that distributed requires memory on all dies. Note that it will always be at the top of DRAM if some dies do not have memory regardless of this option's setting. Also, Consolidation to 1st DRAM pair is only valid in the non-interleaved case.			
			▶Auto	Distributed	Consolidated	
		CXL Memory interleaving	Allows for enabling/disabling CXL memory devices interleaving.			
			▶Auto	Enabled	Disabled	
		CXL Sublink interleaving	Enable or disable CXL sublink interleaving.			
			▶Auto	Enable	Disable	

DF Common Options	ACPI	ACPI SRAT L3 Cache As NUMA Domain	Enabled: Each CCX in the system will be declared as a separate NUMA domain. Disabled: Memory Addressing \ NUMA nodes per socket will be declared.			
			▶Auto	Enabled	Disabled	
		ACPI SLIT Distance Control	Determines how the SLIT distances are declared.			
			▶Auto	Manual		
		ACPI SLIT remote relative distance	Set the remote socket distance for 2P systems as near (2.8) or far (3.2).			
			▶Auto	Near	Far	
	Link	GMI encryption control	Control GMI link encryption.			
			▶Auto	Enabled	Disabled	
		xGMI encryption control	Control xGMI link encryption.			
			▶Auto	Enabled	Disabled	
		xGMI Link Configuration	Configures the number of xGMI2 links used on a multi-socket system.			
			▶Auto	3 xGMI Links	4 xGMI Links	2 xGMI Links+ 2 PCI Links
		4-link xGMI max speed	Specifies the max frequency used for XGMI PState in a 4-link topology.			
			▶Auto	20Gbps	25Gbps	32Gbps
		3-link xGMI max speed	Specifies the max frequency used for XGMI PState in a 3-link topology.			
			▶Auto	20Gbps	25Gbps	32Gbps
		xGMI 18GACOFC	xGMI 18GACOFC control.			
			▶Auto	Enable	Disable	
		xGMI CRC Scale	Configure leaky bucket scale for xGMI and WAFL CRC errors. Every scale milliseconds an error will leak from the CRC counter.			
			5			
		xGMI CRC Threshold	Configure leaky bucket threshold for xGMI and WAFL CRC errors. If link CRC counter exceeds this threshold, an error will be logged.			
			25			
		xGMI Preset Control	Enable/Disable XGMI Preset Control options.			
			Auto		▶Enabled	Disabled
		xGMI Global Preset List	Preset P11	Preset P11 Cmn1	Enable/Disable Preset P11 Cmn1 option on xGMI Global Preset List.	
					0	
				Preset P11 Cn	Enable/Disable Preset P11 Cn option on xGMI Global Preset List.	
					30	
				Preset P11 Cnp1	Enable/Disable Preset P11 Cnp1 option on xGMI Global Preset List.	
					0	
			Preset P12	Preset P12 Cmn1	Enable/Disable Preset P12 Cmn1 option on xGMI Global Preset List.	
					0	
				Preset P12 Cn	Enable/Disable Preset P12 Cn option on xGMI Global Preset List.	
					30	
				Preset P12 Cnp1	Enable/Disable Preset P12 Cnp1 option on xGMI Global Preset List.	
					0	
			Preset P13	Preset P13 Cmn1	Enable/Disable Preset P13 Cmn1 option on xGMI Global Preset List.	
					0	
				Preset P13 Cn	Enable/Disable Preset P13 Cn option on xGMI Global Preset List.	
					30	

DF Common Options	Link	xGMI Global Preset List	Preset P13	Preset P13 Cnp1	Enable/Disable Preset P13 Cnp1 option on xGMI Global Preset List. 0
			Preset P14	Preset P14 Cmn1	Enable/Disable Preset P14 Cmn1 option on xGMI Global Preset List. 0
				Preset P14 Cn	Enable/Disable Preset P14 Cn option on xGMI Global Preset List. 30
				Preset P14 Cnp1	Enable/Disable Preset P14 Cnp1 option on xGMI Global Preset List. 0
			Preset P15	Preset P15 Cmn1	Enable/Disable Preset P15 Cmn1 option on xGMI Global Preset List. 0
				Preset P15 Cn	Enable/Disable Preset P15 Cn option on xGMI Global Preset List. 30
				Preset P15 Cnp1	Enable/Disable Preset P15 Cnp1 option on xGMI Global Preset List. 0
		xGMI Initial Preset	Initial Preset Socket 0 Link 0	Initial Preset Socket 0 Link 0 Pstate 0-3	Enable/Disable Initial Preset Socket 0 Link 0 Pstate 0-3 4
			Initial Preset Socket 0 Link 1	Initial Preset Socket 0 Link 1 Pstate 0-3	Enable/Disable Initial Preset Socket 0 Link 1 Pstate 0-3 4
			Initial Preset Socket 0 Link 2	Initial Preset Socket 0 Link 2 Pstate 0-3	Enable/Disable Initial Preset Socket 0 Link 2 Pstate 0-3 4
			Initial Preset Socket 0 Link 3	Initial Preset Socket 0 Link 3 Pstate 0-3	Enable/Disable Initial Preset Socket 0 Link 3 Pstate 0-3 4
			Initial Preset Socket 1 Link 0	Initial Preset Socket 1 Link 0 Pstate 0-3	Enable/Disable Initial Preset Socket 1 Link 0 Pstate 0-3 4
			Initial Preset Socket 1 Link 1	Initial Preset Socket 1 Link 1 Pstate 0-3	Enable/Disable Initial Preset Socket 1 Link 1 Pstate 0-3 4
			Initial Preset Socket 1 Link 2	Initial Preset Socket 1 Link 2 Pstate 0-3	Enable/Disable Initial Preset Socket 1 Link 2 Pstate 0-3 4
			Initial Preset Socket 1 Link 3	Initial Preset Socket 1 Link 3 Pstate 0-3	Enable/Disable Initial Preset Socket 1 Link 3 Pstate 0-3 4
		xGMI TXEQ Search Mask	TXEQ Search Mask Socket 0 Link 0	TXEQ Search Mask Socket 0 Link 0 Pstate 0-3	Enable/Disable TXEQ Search Mask Socket 0 Link 0 Pstate 0-3 7A
			TXEQ Search Mask Socket 0 Link 1	TXEQ Search Mask Socket 0 Link 1 Pstate 0-3	Enable/Disable TXEQ Search Mask Socket 0 Link 1 Pstate 0-3 7A

DF Common Options	Link	xGMI TXEQ Search Mask	TXEQ Search Mask Socket 0 Link 2	TXEQ Search Mask Socket 0 Link 2 Pstate 0-3	Enable/Disable TXEQ Search Mask Socket 0 Link 2 Pstate 0-3			
					7A			
			TXEQ Search Mask Socket 0 Link 3	TXEQ Search Mask Socket 0 Link 3 Pstate 0-3	Enable/Disable TXEQ Search Mask Socket 0 Link 3 Pstate 0-3			
					7A			
			TXEQ Search Mask Socket 1 Link 0	TXEQ Search Mask Socket 1 Link 0 Pstate 0-3	Enable/Disable TXEQ Search Mask Socket 1 Link 0 Pstate 0-3			
					7A			
			TXEQ Search Mask Socket 1 Link 1	TXEQ Search Mask Socket 1 Link 1 Pstate 0-3	Enable/Disable TXEQ Search Mask Socket 1 Link 1 Pstate 0-3			
					7A			
			TXEQ Search Mask Socket 1 Link 2	TXEQ Search Mask Socket 1 Link 2 Pstate 0-3	Enable/Disable TXEQ Search Mask Socket 1 Link 2 Pstate 0-3			
					7A			
			TXEQ Search Mask Socket 1 Link 3	TXEQ Search Mask Socket 1 Link 3 Pstate 0-3	Enable/Disable TXEQ Search Mask Socket 1 Link 3 Pstate 0-3			
					7A			
		xGMI AC/DC Coupled Link	xGMI AC/DC Coupled Link Control	Control XGMI AC/DC Coupled Link. Valid value: 0: AC coupled 1: DC coupled				
				►Auto	Manual			
		xGMI Channel Type	xGMI Channel Type Control	Control xGMI Channel Type. Valid channel type: 0: Disabled 1: Long Reach				
				►Auto	Manual			
		xGMI Training Err Mask	Enable/Disable XGMI training err mask.					
			►Auto	Enable	Disable			
	SDCI	SDCI	Enable/Disable Smart Data Cache Injection feature.					
			►Auto	Enabled	Disabled			
	Probe Filter	Organization	Specifies whether multiple memory/CXL channels will share probe filter storage. For memory sizes of 16TB or larger, this feature is ignored as it is auto-selected to 'shared'					
			Auto	►Dedicated	Shared			
		Periodic Directory Rinse (PDR) Tuning	Controls PDR settings that may impact performance by workload and/or processor. Memory-Sensitive: May accelerate high b/w scenarios Cache-Bound: May accelerate cache-bound scenarios Neutral: Fallback option for unknown or mixed scenarios Adaptive: Adjusts based on Memory/Cache Activity.					
			►Auto	Memory-Sensitive	Cache-Bound	Neutral	Adaptive	
	DF Watchdog Timer Interval		Configure the Data Fabric watchdog timer interval.					
			►Auto	41 ms	166 ms	334 ms		
			669 ms	1.34 seconds	2.68 seconds	5.36 seconds		
	Disable DF to external IP SyncFloodPropagation		Disable SyncFlood to UMC & downstream slaves.					
			►Auto	Sync flood enabled	Sync flood disabled			
	Sync Flood Propagation to DF Components		Control DF::PIEConfig[DisSyncFloodProp]					
			►Auto	Sync flood enabled	Sync flood disabled			

DF Common Options	Freeze DF module queues on error		Controls DF::PIEConfig[DisImmSyncFloodOnFatalError] Disabling this option sets DF:PIEConfig[DisImmSyncFloodOnFatalError]						
			►Auto	Enabled	Disabled				
	CC6 memory region encryption		Control whether or not the CC6 save/restore memory is encrypted.						
			►Auto	Enabled	Disabled				
	CCD B/W Balance Throttle Level		Enables throttling of memory traffic per CCD. Increased throttling can reduce imbalance across CCDs (expected to be rare).						
			►Auto	Level 0	Level 1	Level 2	Level 3	Level 4	
	P2P Ordered Writes		When set to Disabled, ordering of P2P writes targeting multiple end points is no longer guaranteed by the host.						
			►Enabled	Disabled					
UMC Common Options	DDR Addressing Options	Chipselect Interleaving	Interleave DRAM accesses across ranks within a memory channel if the configuration supports it. 'Enable' will override certain optimization policies, but cannot force interleaving on configurations that do not support it.						
			►Auto	Enabled	Disabled				
		Address Hash Bank	Enable/disable bank address hashing.						
			►Auto	Enabled	Disabled				
		Address Hash CS	Enable/disable CS address hashing.						
			►Auto	Enabled	Disabled				
		Address Hash RM	Enable/disable RM address hashing for 3DS DIMMs.						
			►Auto	Enabled	Disabled				
		Address Hash Subchannel	Enable/disable sub-channel address hashing.						
			►Auto	Enabled	Disabled				
		BankSwapMode	BankSwapMode value: 0=Disabled, 1=SwapCPU						
			►Auto	Disabled	Swap CPU				
	DDR Controller Configuration	DDR Power Options	Power Down Enable	Enable/disable DDR power down mode.					
				►Auto	Enabled	Disabled			
			Sub Urgent Refresh Lower Bound	Specifies the stored refresh limit required to enter sub-urgent refresh mode Constraint: SubUrgRefLowerBound <= UrgRefLimit Valid value: 6 ~ 1					
				1					
			Urgent Refresh Limit	Specifies the stored refresh limit required to enter urgent refresh mode Constraint: SubUrgRefLowerBound <= UrgRefLimit Valid value: 6 ~ 1					
				4					
			DRAM Refresh Rate	DRAM refresh rate: 1.95us or 3.9us (default)					
				►3.9 usec	1.95 usec				
			Self-Refresh Exit Staggering	Tcksrx += (Trfc/n * (UMC_Number % 3)) Selectable by CBS Option: Disable Staggering n = 1 <= Stagger Channels by ~270 ns n = 2 n = 3 n = 4 . . . n = 9 <= Stagger Channels By ~30 ns (Default)					
				Disabled	n= 1	n= 2	n= 3	n= 4	
				n= 5	n= 6	n= 7	n= 8	►n= 9	

UMC Common Options	DDR Controller Configuration	Memory Channel Disable	Memory Channel Disable Float Power Good	Float Power Good when channel is disabled by BIOS setup options.			
				Enabled	▶Disabled		
			Socket 0 Channel 0-11	SPD reading will be skipped when channel is disabled.			
				▶Enabled	Disabled		
			Socket 1 Channel 0-11	SPD reading will be skipped when channel is disabled.			
				▶Enabled	Disabled		
		Refresh Management (RFM)	Refresh Management	Auto: Disable Disable: Disable RFM for all Ranks. Enable: Enable RFM for Ranks which support RFM. Force Enable: Enable RFM for all Ranks regardless of support. Selecting 'Force Enable' will cause REFpb/ REFsb to be disabled if all ranks do not support RFM			
				▶Auto	Disable	Enable	Force Enable
			RAA Initial Management Threshold	Override Rolling Accumulated ACT Initial Management Threshold Auto: BIOS will choose the lowest supported value from SPD. Choices from list are for Normal Refresh Mode. In Fine Granularity Mode, the value will be divided by 2.			
				▶Auto	32	40	48
				56	64	72	80
			RAA Maximum Management Threshold	Override Rolling Accumulated ACT Maximum Management Threshold Auto: BIOS will choose the lowest supported value from SPD. Choices from list are for Normal Refresh Mode. In Fine Granularity Mode, the value will be divided by 2.			
				▶Auto	3X	4X	5X	6X
			RAA Refresh Decrement Multiplier	Override RAA Refresh Decrement Multiplier Auto: BIOS will choose the lowest supported value from SPD.			
				▶Auto	0.5	1	
	DDR MBIST Options	MBIST Enable	Enable/Disable Memory MBIST.				
			▶Auto	Enabled	Disabled		
		Data Eye	Pattern Select	MBIST Data Eye Pattern Type. 0 - PRBS (default) 1 - SSO 2 - Both			
				▶PRBS	SSO	Both	
			Pattern Length	This token determine the pattern length, available options: 3...C (input hex number, not decimal).			
				3			
			Aggressor Channel	One Sub-Channel enables the non-target subchannel on the target channel to be an aggressor. Half Channels enables all non-target channels on one half of the processor to be aggressors. All Channels enables all non-target channels to be aggressors..			
				One Sub-Channel	Half Channels	▶All Channels	

UMC Common Options	DDR MBIST Options	Data Eye	Aggressor Static Lane Control	This option, if enabled, will control the Aggressor Static Lane Controls. ▶Disabled | Enabled
			Target Static Lane Control	Enable Mbist Target Static Lane Control. ▶Disabled | Enabled
			Worst Case Margin Granularity	Mbist Worst Case Margin Granularity 0 = Per Chip Select 1 = Per Nibble ▶Per Chip Select | Per Nibble
			Read Voltage Sweep Step Size	This option determines the step size for Read Data Eye voltage sweep, Supported options are 1,2 and 4. ▶1 | 2 | 4
			Read Timing Sweep Step Size	This options supports step size for Read Data Eye. Supported options are 1, 2 and 4. ▶1 | 2 | 4
			Write Voltage Sweep Step Size	This option determines the step size for write Data Eye voltage sweep, Supported options are 1,2 and 4. ▶1 | 2 | 4
			Write Timing Sweep Step Size	This options supports step size for write Data Eye. Supported options are 1, 2 and 4. ▶1 | 2 | 4
			Silent Execution	Execute MBIST Data Eye silently without ABL log output. Disabled- MBIST Enable will not be overridden Enabled- Execute MBIST Data Eye silently without ABL log output. ▶Disabled | Enabled
		DDR Healing BIST		This item enables a full memory test. Please note that this is a memory content test and is separate and distinct from the MBIST test of Interface and Data Eye. PMU Mem BIST: this uses PMU firmware to test memory on all channels simultaneously. Failing memory will be repaired using soft or hard PPR depending on the PPR configuration. Self-Healing Mem BIST: this runs the JEDEC DRAM self healing, if the device and DIMM support the feature. The DRAM will do a hard repair for failing memory. PMU and Self-Healing Mem BIST: this option runs the PMU Mem BIST then the Self-Healing Mem BIST tests sequentially. ▶Disabled | PMU Mem BIST | Self-Healing Mem BIST | PMU and Self-Healing Mem BIST
	DDR RAS	Data Poisoning		Enable poison data creation on uncorrectable DDR DRAM ECC errors and poison propagation to CPU cores and caches. Requires ECC memory. When FALSE, a fatal error event will occur on DDR ECC errors sets UMC_CH::EccCtrl[UcFatalEn] when MC_CH::EccCtrl[WrEccEn] is set. Auto | Enabled | ▶Disabled
		DRAM Boot Time Post Package Repair		Enable/Disable DRAM Boot Time Post Package Repair. ▶Disable | Enable
		DRAM Runtime Post Package Repair		Enable/Disable DRAM Run Time Post Package Repair. ▶Disable | Enable

UMC Common Options	DDR RAS	RCD Parity	Enable RCD command and address parity.					
			Auto	▶Enabled	Disabled			
		Max RCD Parity Error Replay	Program to UMC::RecCtrl[MaxParRply], valid value:1 - 3F hex, default 8.					
			8					
		Disable Memory Error Injection	0=Enable. 1=Disable. Specifies UMC error injection configuration writes are disabled. True: UMC::CH::MiscCfg[DisErrInj]=1					
			▶Auto	True	False			
		ECC Configuration	DRAM ECC Symbol Size	DRAM ECC Symbol Size (x4/x16) - UMC_CH::EccCtrl[EccSymbolSize16, EccSymbolSize]				
				▶Auto	x4	x16		
			DRAM ECC Enable	Use this option to enable / disable DRAM ECC. Auto will set ECC to enable.				
				▶Auto	Enabled	Disabled		
			DRAM UECC Retry	DRAM UECC Retry. Program to UMC::RecCtrl.RecEn [2]				
				Auto	Enabled	▶Disabled		
			Memory Clear	Clear/Zero out Dram range [DramScrubBaseAddr: DramScrubLimitAddr].When this option is disabled, Memory is not cleared after training. ECC Dimms have memory clear enabled always. Non-ECC Dimms can choose to disable/enable using this option. Default = Memclear enabled				
				▶Auto	Enabled	Disabled		
			Address XOR after ECC	In order to provide data integrity when data is returned from the wrong address, UMC will hash the data after ECC with the normalized address.				
				▶Auto	Enabled	Disabled		
		DRAM Scrubbers	DRAM ECS Mode	0 = AutoECS Mode 1 = ManualECS mode				
				▶Auto	Auto-mati-cECS	Man-ualECS	DisableECS	
			DRAM Redi-rect Scrubber Enable	Enable/Disable Dram Redirect Scrubber.				
				▶Auto	Enabled	Disabled		
			DRAM Scrub Redirection Limit	Dram ECC Scrub Redirection Limit:0=8 scrubs, 1=4 scrubs, 2=2 scrubs, 3=1 scrub				
				▶Auto	8 scrubs	4 scrubs	2 scrubs	1 scrub
			DRAM Scrub Time	Provide a value that is the number of hours to scrub memory.				
				Disabled	1 hour	4 hour	6 hour	8 hour
				12 hour	16 hour	▶24 hour	48 hour	
			DRAM Error Threshold Count	List of Values: 0 = ETC_4, 1 = ETC_16, 2 = ETC_64, 3 = ETC_256 (default - Auto), 4 = ETC_1024, 5 = ETC_4096				
				▶Auto	ETC_4	ETC_16	ETC_64	
				ETC_256	ETC_1024	ETC_4096		

UMC Common Options	DDR RAS	DRAM Scrubbers	DRAM ECS Count Mode	0: RowCount Mode 1: CodeWord Mode 0xFF: Auto - ABL decides default as CodeWord Mode			
				Row Count Mode	Code Word Count Mode	▶Auto	
			DRAM AutoEcs during Self Refresh	0: AutoEcs Disabled 1: AutoEcs Enabled 0xFF: Auto - ABL choose AutoEcs Disabled			
				AutoEcs Disabled	AutoEcs Enabled	▶Auto	
			DRAM ECS WriteBack Suppression	To enable/Disable ECS Error Correction Writeback suppression 0: ECS Writeback Suppression Disabled 1: ECS Writeback Suppression Enabled 0xFF: Auto - ABL chooses Writeback Suppression to be Enabled by default			
				▶Auto	Enable	Disable	
			DRAM X4 WriteBack Suppression	To enable/Disable X4 device Error Correction Writeback suppression 0: X4 Writeback Suppression Disabled 1: X4 Writeback Suppression Enabled 0xFF: Auto			
				▶Auto	Enable	Disable	
		DRAM Corrected Error Counter Enable	Configure DRAM Corrected Error Counter function. Only meaningful when PcdAmdCcxCfgPFEHEnable is TRUE.				
			Disable	NoLeakMode	▶LeakMode		
		DRAM Corrected Error Counter Interrupt Enable	Enable SMI when DRAM Corrected Error Counter count exceeds the threshold value.				
			▶True	False			
		DRAM Corrected Error Counter Leak Rate	Program Rate value for DRAM Corrected Error Counter function. Only meaningful when PcdAmdDdrEccErrorCounterEnable is set to LeakMode (Value :0x00-0x1F).				
			7				
		DRAM Corrected Error Counter Start Count	Program starting count value for DRAM Corrected Error Counter function. Only meaningful when PcdAmdDdrEccErrorCounterEnable is not Disable (0x00 - 0xFFFF).				
			FFF5				
	DDR Bus Configuration	Dram ODT impedance RTT_NOM_WR	Select the DRAMs On-die Termination impedance for RTT_NOM_WR.				
			▶Auto	RTT_OFF	RZQ(240)	RZQ/2 (120)	RZQ/3 (80)
			RZQ/4 (60)	RZQ/5 (48)	RZQ/6 (40)	RZQ/7 (34)	
		Dram ODT impedance RTT_NOM_RD	Select the DRAMs On-die Termination impedance for RTT_NOM_WR.				
			▶Auto	RTT_OFF	RZQ(240)	RZQ/2 (120)	RZQ/3 (80)
			RZQ/4 (60)	RZQ/5 (48)	RZQ/6 (40)	RZQ/7 (34)	
		Dram ODT impedance RTT_WR	Select the DRAMs On-die Termination impedance for RTT_WR.				
			▶Auto	RTT_OFF	RZQ(240)	RZQ/2 (120)	RZQ/3 (80)
			RZQ/4 (60)	RZQ/5 (48)	RZQ/6 (40)	RZQ/7 (34)	

UMC Common Options	DDR Bus Configuration	Dram ODT impedance RTT_PARK	Select the DRAMs On-die Termination impedance for RTT_PARK.				
			▶Auto	RTT_OFF	RZQ(240)	RZQ/2 (120)	RZQ/ 3 (80)
			RZQ/ 4 (60)	RZQ/ 5 (48)	RZQ/ 6 (40)	RZQ/ 7 (34)	
		Dram ODT impedance DQS_RTT_PARK	Select the DRAMs On-die Termination impedance for DQS_RTT_PARK.				
			▶Auto	RTT_OFF	RZQ(240)	RZQ/2 (120)	RZQ/ 3 (80)
			RZQ/ 4 (60)	RZQ/ 5 (48)	RZQ/ 6 (40)	RZQ/ 7 (34)	
		Processor ODT impedance	Select the ODT impedance for all DBYTE IOs.				
			▶Auto	High Impedance	480 ohm	240 ohm	160 ohm
			120 ohm	96 ohm	80 ohm	68.6 ohm	60 ohm
			53.3 ohm	48 ohm	43.6 ohm	40 ohm	36.9 ohm
			34.3 ohm	32 ohm	30 ohm	28.2 ohm	26.7 ohm
			25.3 ohm				
		Dram DQ drive strengths	Selects the Dram Pull-up and Pull-Down Output Driver Impedance for all DQ and DMI IOs.				
			▶Auto	48 ohm	40 ohm	34 ohm	
	DDR Timing Configuration	Decline					
		Accept	Active Memory Timing Settings	Active Memory Timing Settings.			
				Auto	▶Enabled		
			Memory Target Speed	Specifies the memory target speed in MT/s.			
				▶Auto	DDR3600	DDR4000	DDR4400
				DDR4800	DDR5200	DDR5600	
			SPD Timing	Tcl Ctrl/Trcd Ctrl/Trp Ctrl/Tras Ctrl/Trc Ctrl/Twr Ctrl/Trfc1 Ctrl/Trfc2 Ctrl/TrfcSb Ctrl			Auto: Follow default setting Manual: Manually specify
							▶Auto / Manual
			Non-SPD Timing	Tcwl Ctrl/Trtp Ctrl/TrrdL Ctrl/ Trrds Ctrl/Tfaw Ctrl/ TwtrL Ctrl/TwtrS Ctrl/TrdrdScL Ctrl/TrdrdSc Ctrl/TrdrdSd Ctrl/ TrdrdDd Ctrl/TwrwrScL Ctrl/ TwrwrSc Ctrl/TwrwrSd Ctrl/ TwrwrDd Ctrl/Twrrd Ctrl/ Trdwr Ctrl			Auto: Follow default setting Manual: Manually specify
							▶Auto / Manual
	DDR Training Options	DRAM PDA Enumerate ID Programming Mode	Specify PDA enumeration mode Auto : default 0 : Continuous DQS toggling PDA enumeration mode (default) 1 : Legacy PDA enumeration mode				
			▶Auto	Toggling PDA enumeration mode	Legacy PDA enumeration mode		
		Training Retry Count	Retry on PMU training failure, retry to all channels, including passed and failed channel. Input value in decimal. 0: skip retry.				
			8				
	DDR Security	TSME	Transparent SME				
			▶Auto	Enabled	Disabled		
		AES	AES mode: AES-128 or AES-256 (default)				
			AES-128	▶AES-256			

UMC Common Options	DDR Security	Data Scramble	Data scrambling: DataScrambleEn ▶Enabled | Disabled
		SME-MK	SME-MK encryption mode. Enabling both SMEE and SME-MK is not supported. Results in #GP. Enabled | ▶Disabled
	DDR PMIC Configuration	PMIC Error Reporting	Enables support for PMIC Error Reporting. ▶Auto | True | False
		PMIC Operation Mode	1 - Programmable Mode Operation (default); 0 - Secure Mode Operation Programmable mode allows certain registers to be programmed after VR enable else they will be in secure mode Secure Mode | ▶Programmable Mode
		PMIC Fault Recovery	0 - Always; 1 - Never (default); 2 - Once Always - PMIC will ignore previous boot errors. No channel disabled Never - PMIC disables the channel with errors from previous boot. Once - PMIC will disable the channel if more than one error is detected on previous boot, else it is ignored. ▶Always | Never | Once
		PMIC SWC VDDIO	Range is from 1000mV to 1200mV; default of 1100mV. 1100
		PMIC SWA/SWB VDD Core	Range is from 1000mV to 1200mV; default of 1100mV. 1100
		PMIC Stagger Delay	Amount of time to wait between powering on DIMMs in milliseconds. 5
		Max PMIC Power On	Maximum number of DIMMs that can power on at the same time. FF
	DDR Miscellaneous	DRAM Survives Warm Reset	1 - Enabled (default); 0 - Disabled If enabled - Upon warm reset DRAM content is preserved, Training values are saved & retrieved. Enabled | ▶Disabled
		ODTS CMD Throttle Threshold	Dram MR4 Temperature status value to start ODTS Command Thermal Throttlling. ▶Auto | > 85'C | > 90'C | > 95'C
		Vendor specific RCD workaround	Workaround a specific I2C/I3C switching issue with a specific DIMM SPD hub vendor. Enabled | ▶Disabled
	DDR PHY (CMN)	Periodic Training	Specifies Periodic Training config. ▶Auto | Enabled | Disabled
NBIO Common Options	IOMMU		Enable/Disable IOMMU. ▶Auto | Enabled | Disabled
	DMAr Support		Enable DMAr system protection during POST. ▶Auto | Enabled | Disabled
	DMA Protection		Enable DMA remap support in IVRS IVinfo Field. ▶Auto | Enabled | Disabled
	DRTM Virtual Device Support		Enable DRTM ACPI virtual device. ▶Auto | Enabled | Disabled
	DRTM Memory Reservation		Reserve 128MB memory below Bottom IO for DRTM. It is required to be enabled for Secured-Core Server function. ▶Auto | Enabled | Disabled
	ACS Enable		AER must be enabled for ACS enable to work. ▶Auto | Enable | Disabled

NBIO Common Options	PCIe ARI Support	Enables Alternative Routing-ID Interpretation.			
		▶Auto	Enable	Disable	
	PCIe ARI Enumeration	ARI Forwarding Enable for each downstream port.			
		▶Auto	Enable	Disable	
	PCIe Ten Bit Tag Support	Enables PCIe ten bit tags for supported devices.			
		▶Auto	Enable	Disable	
	Low Latency NIC Fast Mode Support	Enable/Disable Low Latency NIC Fast Mode Support.			
		▶Auto	Enable	Disable	
	SMU Common Options	TDP Control	Auto = Use the fused TDP Manual = User can set customized TDP		
			▶Auto	Manual	
		PPT Control	Auto = Use the fused PPT Manual = User can set customized PPT		
			▶Auto	Manual	
		Determinism Control	Auto = Use default performance determinism settings Manual = User can set custom performance determinism settings		
			▶Auto	Manual	
		xGMI Link Width Control	Auto = Use default xGMI link width controller settings Manual = User can set custom xGMI link width controller settings		
			▶Auto	Manual	
		APBDIS	0 = not APBDIS (mission mode) 1 = APBDIS		
			▶Auto	0	1
		DfPstate Range Support	DF Pstate selection is overridden by the APB_DIS BIOS option if it is selected. If enable this feature, the range value setting should follow the rule that MaxDfPstate <= MinDfPstate. Otherwise it will not work.		
			▶Auto	Enable	Disable
		Power Profile Selection	DF Pstate selection in the profile policy is overridden by the pstate range BIOS option or the APB_DIS BIOS option if either one is selected. [0 = High Performance Mode (DEFAULT); 1 = Efficiency Mode; 2 = Maximum IO Performance Mode]			
			▶High Performance Mode	Efficiency Mode	Maximum IO Performance Mode	Balanced Memory Performance Mode
		BoostFmaxEn	Auto = Use the default Fmax Manual = User can set the boost Fmax		
			▶Auto	Manual	
		DF PState Frequency Optimizer	Disabled - means disable the DFPstate CCLK effective frequency optimizer Enabled - means enable the DFPstate CCLK effective frequency optimizer		
			▶Auto	Enabled	Disabled
		DF Cstates	Enable = Enable the feature : Disable = Disable the feature		
			▶Auto	Enabled	Disabled
		CPPC	Enable = Enable the feature : Disable = Disable the feature		
			▶Auto	Enabled	Disabled
		HSMP Support	Select HSMP support enable or disable.		
			▶Auto	Enabled	Disabled

NBIO Common Options	SMU Common Options	SVI3 SVC Speed Control	No help string			
			▶Auto	Manual		
		Diagnostic Mode	Select Diag mode enable or disable.			
			▶Auto	Enabled	Disabled	
		PCIE Speed PMM Control	Reduce link speed when devices are idle.			
			▶Auto	Dynamic link speed determined by Power Management functionality	Static Target Link Speed (GEN4)	Static Target Link Speed (GEN5)
	NBIO RAS Common Options	NBIO RAS Control	(0) Disabled, (1) MCA			
			▶Auto	MCA	Disabled	
		Egress Poison Severity High	Each bit set to 1 enables HIGH severity on the associated IOHC egress port. A bit of 0 indicates LOW severity.			
			30011			
		Egress Poison Severity Low	Each bit set to 1 enables HIGH severity on the associated IOHC egress port. A bit of 0 indicates LOW severity.			
			4			
		NBIO SyncFlood Generation	This value may be used to mask SyncFlood caused by NBIO RAS options. When set to TRUE SyncFlood from NBIO is masked. When set to FALSE NBIO is capable of generating SyncFlood.			
			▶Auto	Enabled	Disabled	
		NBIO SyncFlood Reporting	This value may be used to enable SyncFlood reporting to APML. When set to TRUE SyncFlood will be reported to APML. When set to FALSE that reporting well be disabled.			
			▶Auto	Enabled	Disabled	
		Egress Poison Mask High	These set the enable mask for masking of errors logged in EGRESS_POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions.			
			FFFCFFFF			
		Egress Poison Mask Low	These set the enable mask for masking of errors logged in EGRESS_POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions.			
			FFFFFFFB			
		Uncorrected Converted to Poison Enable Mask High	These set the enable mask for masking of uncorrectable parity errors on internal arrays. For each bit set to 1, a system fatal error event is triggered for UCP errors on arrays associated with that egress port. For each bit set to 0, errors are masked.			
			30000			
		Uncorrected Converted to Poison Enable Mask Low	These set the enable mask for masking of uncorrectable parity errors on internal arrays. For each bit set to 1, a system fatal error event is triggered for UCP errors on arrays associated with that egress port. For each bit set to 0, errors are masked.			
			4			
		System Hub Watchdog Timer	This value specifies the timer interval of the SYSHUB Watchdog timer in miliseconds. Maximium value is 5200ms.			
			2600			
		PCIe Aer Reporting Mechanism	This value selects the method of reporting AER errors from PCI Express. A value of 1 allows OS First handling of the errors through generation of a system control interrupt (SCI). A value of 2 provides for Firmware First handling of errors through generation of a system management interrupt (SMI).			
			▶Auto	Firmware First	Firmware First but allow OS First	Os First

NBIO Common Options	NBIO RAS Common Options	Edpc Control	(0) Disabled; (1) Enabled; (3) Auto			
			►Auto	Enabled	Disabled	
		ACS RAS Request Value	No help string.			
			►Auto	Direct Request Access Enabled	Request Blocking Enabled	Request Redirect Enabled
		NBIO Poison Consumption	NBIO Poison Consumption.			
			►Auto	Enabled	Disabled	
		Sync Flood on PCIe Fatal Error	When 'Sync Flood on PCIe Fatal Error' is True, PcdAmdPcieSyncFloodOnFatal should be set to True. When 'Sync Flood on PCIe Fatal Error' is False, PcdAmdPcieSyncFloodOnFatal should be set to False. When 'Sync Flood on PCIe Fatal Error' is Auto, PcdAmdPcieSyncFloodOnFatal should retain its AGESA default.			
			►Auto	True	False	
	Enable AER Cap	Enables Advanced Error Reporting Capability.				
		►Auto	Enable	Disabled		
	Early Link Speed	Set Early Link Speed.				
		►Auto	Gen1	Gen2		
	Hot Plug Handling mode	Control the Hot Plug Handling mode Note: 'Firmware First but allow OS First' is a development mode and not to be used until operating systems with this support are available. SFI mode REQUIRES an operating system that supports DPC. (Most recent Linux operating systems support/enable this)				
		►Auto	OS First	Firmware First/EDR if OS supports	Firmware First but allow OS First	System Firmware Intermediary
	Hot Plug Allow FF in Synchronous	Allows firmware first hot plug handling mode to operate in mode A and mode B synchronous mappings.				
		►Disabled	Enabled			
	Presence Detect Select mode	Control the Presence Detect Select mode.				
		►Auto	OR	AND	In-Band Only	Out-Of-Band Only
	Data Link Feature Cap	Data Link Feature Capability.				
		►Auto	Enabled	Disabled		
	CV test	Set this to Enabled to support running PCIECV tool. Auto - preserve h/w defaults.				
		►Auto	Enabled	Disabled		
	SEV-SNP Support	Enables support for Secure Encrypted Virtualization and Secure Nested Paging.				
		►Auto	Enable	Disable		
	Allow Compliance	When enabled, allows the PCIe RP to enter Polling.Compliance state.				
		►Auto	Enable	Disable		
	SRIS	SRIS				
		►Auto	Enable	Disable		
	Multi upstream Auto Speed Change	Defines the setting of this feature for all PCIe devices. 'Auto' uses the DXIO default setting of 0 for Gen1 and 1 for Gen2/3.				
		►Auto	Enabled	Disabled		
	Multi Auto Speed Change On Last Rate	Force PCIe link training speed to last advertised for all ports. Disabled=Use highest data rate ever advertised. Enabled=Use last data rate advertised.				
		►Auto	Enable	Disable		
	PCIE Link Speed Capability	Set all PCIe port speed capability				
		►Auto	Maximum speed	Gen1	Gen2	
		GEN3	GEN4	GEN5		
	RTM Margining Support	RTM Margining Support.				
		►Auto	Enable	Disable		

NBIO Common Options	EQ Bypass To Highest Rate	Controls the ability to advertise Equalization Bypass to Highest Rate Support in TSxs sent prior to LinkUp=1				
		▶Auto		Enable	Disable	
	Non-PCIe Compliant Support	Enable this setting to send command to disable Extended EIEOS, DLF, and Gen 5 Support on training failure for non-pcie compliant devices.				
		▶Auto		Enable	Disable	
	PCIE Idle Power Setting	Modify PCIE Power Savings Features that Can Impact Lightly Loaded Latency.				
		Optimize for Latency		▶Optimize for Perf/Power		
	nBif Common Options	MPDMA-TF	SRIOV	SRIOV capability Enablement for Pcie capability enablement. STRAP_SRIOV_EN_DEV0_F1[0]		
				▶Auto	Enable	Disable
			ARI	Enable ARI cap in EP function for Pcie capability enablement. STRAP_ARI_EN_DEV0_F1[15]		
				▶Auto/Default	Enable	Disable
			AER	EnableAER cap in EP function for Pcie capability enablement. STRAP_AER_EN_DEV0_F1[16]		
				▶Auto	Enable	Disable
			ACS	Enable ACS cap in EP function for Pcie capability enablement. STRAP_ACS_EN_DEV0_F1[17]		
				▶Auto	Enable	Disable
			ATS	Enable ATS cap in EP function for Pcie capability enablement. STRAP_ATS_EN_DEV0_F1[18]		
				▶Auto	Enable	Disable
			PASID	Enable PASID capability in EP function for Pcie capability enablement. STRAP_PASID_EN_DEV0_F1 [28]		
				▶Auto	Enable	Disable
			RTR	Enable RTR capability in EP function for Pcie capability enablement. STRAP_RTR_EN_DEV0_F1[31]		
				▶Auto	Enable	Disable
			PAGE_REQ	Enable Page request capability in EP function for Pcie capability enablement. STRAP_PAGE_REQ_EN_DEV0_F1[27]		
				▶Auto	Enable	Disable
			PWR	Enable PWR budget capability for Pcie capability enablement. STRAP_PWR_EN_DEV0_F1 [17]		
				▶Auto	Enable	Disable
			ATC_ ENABLE	Enable ATC enable for Pcie ATS Control.PCIE_ ATS_CNTL_dev0_func1 (in the instance nbio NBIF0, nbio0 NBIF1, nbio1 NBIF0, nbio1 NBIF1). ATC_ENABLE [15]		
				▶Auto	Enable	Disable
			SDXI Class Code	Program SDXI specific Class code.		
				▶Auto	Enable	Disable
			PASID Control	ATS Control register, controls if the function is permitted to send requests that contain a PASID value.		
				▶Auto	Enable	Disable
			ATOMICOP _REQUEST	Controls the ability of a function to initiate AtomicOp requests.		
				▶Auto	Enable	Disable

NBIO Common Options	nBif Common Options	RCC_DEV0	ACS Rcc_Dev0	Enable ACS enable for RCC_DEV0 , STRAP_ACS_EN_DN_DEV0		
				►Auto	Enable	Disable
			AER Rcc_Dev0	Enable AER enable for RCC_DEV0 , STRAP_AER_EN_DN_DEV0		
				►Auto	Enable	Disable
			DlfEnableStrap1	RCC_BIF_STRAP1,STRAP_DLF_EN=1		
				►Auto	Enable	Disable
			Phy16GTStrap1	RCC_BIF_STRAP1 ,STRAP_PHY_16GT_EN=1		
				►Auto	Enable	Disable
			MarginEnStrap1	RCC_BIF_STRAP1 ,STRAP_MARGIN_EN=1		
				►Auto	Enable	Disable
			SourceV-alStrap5	RCC_DEV0_PORT_STRAP5 = 0xAF80_0000,Source Validation bit [23]		
				►Auto	Enable	Disable
			Translational-BlockingStrap5	RCC_DEV0_PORT_STRAP5 = 0xAF80_0000,Translational Blocking bit [24]		
				►Auto	Enable	Disable
			P2pReq ACS Control	PCIE_ACS_CNTL_dev0 0x001D,P2P page request bit [2]		
				►Auto	Enable	Disable
			P2pComp-Strap5	RCC_DEV0_PORT_STRAP5 = 0xAF80_0000, P2P Completion bit [26]		
				►Auto	Enable	Disable
			UpstreamFwd-Strap5	RCC_DEV0_PORT_STRAP5 = 0xAF80_0000, Upstream Forwarding bit [27]		
				►Auto	Enable	Disable
			P2PE-gressStrap5	RCC_DEV0_PORT_STRAP5 = 0xAF80_0000, P2P Egress bit [28]		
				►Auto	Enable	Disable
			DirectTrans-latedStrap5	RCC_DEV0_PORT_STRAP5 = 0xAF80_0000,ACS Direct Translated bit [29]		
				►Auto	Enable	Disable
			SsidEnStrap5	RCC_DEV0_PORT_STRAP5 = 0xAF80_0000,ACS SSID Enable bit [31]		
				►Auto	Enable	Disable
			PriEnPageReq	PCIE_PAGE_REQ_CNTL (for all nbio instances) set to 0x0001,PriEn bit set.		
				►Auto	Enable	Disable
			PriResetPag-eReq	PCIE_PAGE_REQ_CNTL (for all nbio instances) set to 0x0001,Pri Reset bit clear.		
				►Auto	Enable	Disable
			SourceVal ACS cntl	PCIE_ACS_CNTL_dev0 = 0x001D, Source Validation bit [0] is set.		
				►Auto	Enable	Disable
			Translational-Blocking ACS Control	PCIE_ACS_CNTL_dev0 = 0x001D, Translational blocking bit [1]		
				►Auto	Enable	Disable
			P2pComp ACS Control	PCIE_ACS_CNTL_dev0=0x001D,P2P Completion bit [3]		
				►Auto	Enable	Disable
			UpstreamFwd ACS Control	PCIE_ACS_CNTL_dev0 = 0x001D,Upstream Forwarding bit [4]		
				►Auto	Enable	Disable

NBIO Common Options	nBif Common Options	RCC_DEV0	P2PEgress ACS Control	PCIE_ACS_CNTL_dev0 = 0x001D,P2P Egress bit [5]			
				►Auto	Enable	Disable	
			P2pReqStrap5	RCC_DEV0_PORT_STRAP5 = 0xAF80_0000,P2P request strap bit.			
				►Auto	Enable	Disable	
			E2E_PREFIX	RCC_DEV0_PORT_STRAP2 has bit STRAP_E2E_PREFIX_EN_DEV0			
				►Auto	Enable	Disable	
			EXTENDED_FMT	RCC_DEV0_PORT_STRAP2 has bit STRAP_EXTENDED_FMT_SUPPORTED_DEV0			
				►Auto	Enable	Disable	
			AtomicRoutingStrap5	NBIF DEV0 Enable AtomicOp Routing support in Downstream Port.			
				►Auto	Enable	Disable	
	Link EQ Preset Options	GEN3-5	Preset Search Mask Configuration (Gen3-5)	Configuration for Gen3-5 Preset Mask. Select Custom to modify Gen3-5 Preset Search Mask. Auto will default to platform configurations.			
				►Auto	Custom		
	Enable 2 SPC (Gen 4)	Enable this setting to use 2 symbols per clock for devices at Gen 4 speed.					
		►Auto		Enable			
	Safe recovery upon a BERExceeded Error	No help string.					
		►Auto		Enable		Disable	
	Periodic Calibration	No help string.					
		►Auto		Enable		Disable	
	Enable PCIe SFI Config via OOB	Enable PCIe SFI Config via OOB support.					
		►True		False			
FCH Common Options	I3C/I2C Configuration Options	I3C/I2C 0-3 Enable		Enable/disable Inter-Integrated Circuit Control 0-3			
				►Auto	Both Disabled	I3C Enabled	I2C Enabled
		I2C 4-5 Enable		Enable/disable Inter-Integrated Circuit Controller4-5			
				►Auto	Enabled	Disabled	
		Release SPD Host Control		Release SPD Host Control, so that BMC can take over the ownership of I2C/I3C bus.			
				Enabled	►Disabled		
		PMFW Poll DDR5 Telemetry		Send message to PMFW for polling DDR5 telemetry at the end of POST.			
				►Enabled	Disabled		
		Ixc Telemetry Ports Fence Control		Controls the Fencing off for I2C/I3C ports which are involved in DDR Telemetry. If this option is enabled, then the associated Ixc ports registers will be put in the secure region. Note: If this option is disabled, there is a risk of collision happening between x86 accessing IxC and PMFW running DDR Telemetry which can cause undefined behavior.			
				Enabled	►Disabled		
		I2C SDA Hold Override		Override I2C SDA_TX_HOLD and SDA_RX_HOLD			
				►Auto	Enabled	Disabled	
		APML SB-TSI & RMI Mode		Select APML SB-TSI over I3C or I2C. In I3C mode, the slave controller can support both I3C and I2C(-Adaptive mode).			
				►I2C	I3C		
		I3C Push Pull HCNT Value		SCL push-pull High count for I3C transfers targeted to I3C devices.			
				8			
		I3C SDA Hold Override		Override I3C SDA HOLD VALUE			
				►Auto	Enabled	Disabled	

FCH Common Options	SATA Configuration Options	SATA Enable	Disable/enable OnChip SATA controller.				
			▶Auto	Enabled	Disabled		
		SATA RAS Support	Disable/enable Sata RAS Support.				
			▶Auto	Enabled	Disabled		
		SATA Staggered Spin-up	Enable/disable SATA staggered spin-up.				
			▶Auto	Enabled	Disabled		
		SATA Disabled AHCI Prefetch Function	Enable/disable Sata Disabled AHCI Prefetch Function.				
			▶Auto	Enabled	Disabled		
		Aggresive SATA Device Sleep P0-P1	Enable SATA DevSlp0-1. In SOC two DEVSLP pads are assigned. Aggressive Device Sleep enables the HBA to assert the DEVSLP signal as soon as there are no commands outstanding to the device and the port specific Device Sleep idle timer has expired.				
			▶Auto	Enabled	Disabled		
		SATA Controller options	SATA Controller Enable	Sata0-3 Enable	Enable/Disable Sata0-3. Each IOD has 4 Sata Controllers.		
					▶Auto	Enabled	Disabled
				Sata4-7 (Socket1) Enable	Enable/Disable Sata4-7 on Socket1(IOD1). Each IOD has 4 Sata Controllers.		
					▶Auto	Enabled	Disabled
			SATA Controller eSATA	SATA Controller eSATA			
			SATA Controller DevSlp	Socket1 DevSlp	Socket1 DevSlp0-1 Enable	Only Sata0 on each IOD/ socket support DevSlp.	
						▶Auto	Enabled	Disabled
			SATA Controller SGPIO	Sata0-3 SGPIO	Enable/Disable SataSgpio on Sata0-3		
					▶Auto	Enabled	Disabled
				Sata4-7 SGPIO	Enable/Disable SataSgpio on Sata4-7 (Socket1)		
					▶Auto	Enabled	Disabled
	USB Configuration Options	XHCI Controller0-1 enable	Enable/disable USB3 controller.				
			Auto	▶Enabled	Disabled		
		USB ecc SMI Enable	Enable Double Error Detection output signal for USB S0 ram.				
			▶Auto	Enabled	Off		
		MCM USB enable	XHCI2-3 enable (Socket1)	Enable/disable USB3 controller.			
				Auto	▶Enabled	Disabled	
	Ac Power Loss Options	Ac Power Loss Options					
	Uart Configuration Options	Uart 0 Enable	Enable/disable Uart0. Uart 0 has no HW flow control if Uart 2 is enabled.				
			▶Auto	Enabled	Disabled		
		Uart 1 Enable	Enable/disable Uart1.				
			▶Auto	Enabled	Disabled		
		Uart 2 Enable	Enable/disable Uart2. If Uart 2 is enable, Uart0 has no HW flow control.				
			▶Auto	Enabled	Disabled		
		Uart 3 Enable	Enable/disable Uart3.				
			▶Auto	Enabled	Disabled		

FCH Common Options	ESPI Configuration Options	ESPI Enable	No help string.		
			▶Auto	Enabled	Disabled
	FCH RAS Options	ALink RAS Support	Enable FCH A-Link parity error.		
			▶Auto	Enabled	Disabled
		Reset After Sync-Flood	Enable AB to forward downstream sync-flood message to system controller.		
			▶Auto	Enable	Disable
	Miscellaneous Options	Boot Timer Enable	Boot Timer enable. Enable : force PMx44 bit 27 = 1 Disable : force PMx44 bit 27 = 0 Auto:PMx44 bit 27 = PcdBootTimerEnable		
			▶Auto	Enabled	Disabled
Soc Miscellaneou -s Control	ABL Console Out Control	Enable : Enable ConsoleOut Function for ABL Disable : Disable ConsoleOut Function for ABL Auto : Keep default behavior			
		▶Auto	Enable	Disable	
	ABL 2nd CPU PMU MsgBlock Log Control	ABL print 2nd CPU PMU MsgBlock contents after training.			
		▶Enabled	Disabled		
	ABL Memory Population message Control	Non-Recommended configurations may be functional but may not be validated by AMD. Select 'warning message': To show warning messages if Memory channel configuration does NOT follow Memory Population Guidelines. 'Fatal error': To show the messages and halt the system.			
		▶Warning message	Fatal error		
	PSP error injection support	Enable EINJ support.			
		True	▶False		
	Firmware Anti-rollback (FAR)	FAR Switch	[Enabled] : BIOS will update SPL fuse to SPL value in the SPL table. [Disabled] : BIOS will not set SPL fuse.		
			▶Auto	Enabled	Disabled
CXL Common Options	CXL Control	Enable/Disable CXL on all ports.			
		▶Auto	Enabled	Disabled	
	CXL SPM	Sets CXL memory as Special Purpose Memory.			
		▶Auto	Enabled	Disabled	
	CXL Encryption	CXL Encryption.			
		Enabled	▶Disabled		
	CXL DVSEC Lock	Locks the CXL DVSEC.			
		▶Auto	Enabled	Disabled	
	Temp Gen5 Advertisement	Temp Gen5 Advertisement for Alternate Protocol.			
		▶Auto	Enable	Disable	
	Sync Header Bypass	Enable/Disable CXL Sync Header Bypass support.			
		▶Auto	Enabled	Disabled	
	CXL RAS	CXL Protocol Error Reporting	Configure CXL Protocol Error reporting mechanism.		
			Disabled	▶SameAsPcieAer	ForceAerFwFirstIfCxlPresent
		CXL Component Error Reporting	Configure CXL Component Error reporting mechanism.		
			Allow OS-First	Force FW-First	▶Debug FW-First
	AckFlushRetimer Configuration	Configure AckFlushRetimer register to revert it back to old value as backup. Configuration 1 will have the register as default value 0x380; Configuration 2 will revert it back to old value 0x100..			
		▶Configuration 1	Configuration 2		

4.4.6 Serial Port Console Redirection

Serial Port Console Redirection

Serial Port Console Redirection		
COM0		
Console Redirection	Console Redirection Enable or Disable.	
	Enabled	▶Disabled
COM1		
Console Redirection	Console Redirection Enable or Disable.	
	Enabled	▶Disabled
COM3		
Console Redirection	Console Redirection Enable or Disable.	
	Enabled	▶Disabled
Console Redirection EMS	Console Redirection Enable or Disable.	
	Enabled	▶Disabled

4.4.7 CPU Configuration

CPU Configuration Parameters.

CPU Configuration		
SVM Mode	Enable/disable CPU Virtualization.	
	▶Enabled	Disabled
Node 0 Information	View Memory Information related to Node 0.	
Node 1 Information	View Memory Information related to Node 1.	

4.4.8 Debug Port Table Configuration

Enable or Disable DBGP and DBG2 Tables.

Debug Port Table Configuration		
Debug Port Table	Debug Port Table	
	Enabled	▶Disabled
Debug Port Table 2	Debug Port Table 2	
	Enabled	▶Disabled

4.4.9 SIO Common Setting

SIO Common Setting.

SIO Configuration		
Lock Legacy Resources	Enables/Disables Lock of Legacy Resources.	
	Enabled	▶Disabled

4.4.10 SIO Configuration

SIO Configuration.

SIO Configuration				
〔*Active*〕Serial Port 1	View and Set Basic properties of the SIO Logical device. Like IO Base, IRQ Range, DMA Channel and Device Mode.			
	Use This Device	Enable/Disable This Logical Device.		
		▶Enabled	Disabled	
	Possible	Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		
		▶Use Automatic Settings	IO=3F8h; IRQ=4; DMA;	IO=3F8h; IRQ=3,4,5,7,9,10,11,12; DMA;
		IO=2F8h; IRQ=3,4,5,7,9,10,11,12; DMA;	IO=3E8h; IRQ=3,4,5,7,9,10,11,12; DMA;	IO=2E8h; IRQ=3,4,5,7,9,10,11,12; DMA;

〔*Active*〕Serial Port 2	View and Set Basic properties of the SIO Logical device. Like IO Base, IRQ Range, DMA Channel and Device Mode.			
	Use This Device	Enable/Disable This Logical Device.		
		▶Enabled	Disabled	
	Possible:	Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		
		▶Use Automatic Settings	IO=2F8h; IRQ=3; DMA;	IO=3F8h; IRQ=3,4,5,7,9,10,11,12; DMA;
		IO=2F8h; IRQ=3,4,5,7,9,10,11,12; DMA;	IO=3E8h; IRQ=3,4,5,7,9,10,11,12; DMA;	IO=2E8h; IRQ=3,4,5,7,9,10,11,12; DMA;
〔*Active*〕Serial Port 3	View and Set Basic properties of the SIO Logical device. Like IO Base, IRQ Range, DMA Channel and Device Mode.			
	Use This Device	Enable/Disable This Logical Device.		
		▶Enabled	Disabled	
	Possible:	Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		
		▶Use Automatic Settings	IO=2E8h; IRQ=7; DMA;	IO=3E8h; IRQ=3,4,5,6,7,10,11,12; DMA;
		IO=2E8h; IRQ=3,4,5,6,7,10,11,12; DMA;	IO=220h; IRQ=3,4,5,6,7,10,11,12; DMA;	IO=228h; IRQ=3,4,5,6,7,10,11,12; DMA;

4.4.11 PCI Subsystem Settings

PCI Subsystem Settings.

PCI Subsystem Settings					
Above 4G Decoding	Globally Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).				
	▶Enabled	Disabled			
Re-Size BAR Support	If system has Resizable BAR capable PCIe Devices, this option Enables or Disables Resizable BAR Support.				
	Enabled	▶Disabled			
SR-IOV Support	If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.				
	▶Enable	Disable			
BME DMA Mitigation	Re-enable Bus Master Attribute disabled during Pci enumeration for PCI Bridges after SMM Locked.				
	Enabled	▶Disabled			
Hot-Plug Support	Globally Enables or Disables Hot-Plug support for the entire System. If System has Hot-Plug capable Slots and this option set to Enabled, it provides a Setup screen for selecting PCI resource padding for Hot-Plug.				
	▶Enabled	Disabled			
JMCIO1/2 Slot Control	Select JMCIO1/2 (CPU0P2) Slot x4x4x4x4 or x8x8 or x16.				
	▶Auto	x4x4x4x4	x8x8	x16	
JMCIO3/4 Slot Control	Select JMCIO3/4 (CPU0P3) Slot x4x4x4x4 or x8x8 or x16.				
	▶Auto	x8x8	x16		
JMCIO5/6 Slot Control	Select JMCIO5/6 (CPU0P1) Slot x4x4x4x4 or x8x8 or x16.				
	▶Auto	x4x4x4x4	x8x8	x16	
JMCIO7/8 Slot Control	Select JMCIO7/8 (CPU0P0) Slot x4x4x4x4 or x8x8 or x16.				
	▶Auto	x4x4x4x4	x8x8	x16	
JMCIO9/10 Slot Control	Select JMCIO9/10 JNGFF1/2 (CPU0G3) x8x4x4 or x4x4x4x4 or x8x8 or x16.				
	▶Auto	x4x4x4x4	x8x4x4	x8x8	x16
JMCIO11/12 Slot Control	Select JMCIO11/12 (CPU1P2) Slot x4x4x4x4 or x8x8 or x16.				
	▶Auto	x4x4x4x4	x8x8	x16	
JMCIO13/14 Slot Control	Select JMCIO13/14 (CPU1P3) Slot x4x4x4x4 or x8x8 or x16.				
	▶Auto	x8x8	x16		
JMCIO15/16 Slot Control	Select JMCIO15/16 (CPU1P1) Slot x4x4x4x4 or x8x8 or x16.				
	▶Auto	x4x4x4x4	x8x8	x16	
JMCIO17/18 Slot Control	Select JMCIO17/18 (CPU1P0) Slot x4x4x4x4 or x8x8 or x16.				
	▶Auto	x4x4x4x4	x8x8	x16	
JMCIO19/20 Slot Control	Select JMCIO19/20 (CPU1G1) x4x4x8 or x4x4x4x4 or x8x8 or x16.				
	▶Auto	x4x4x4x4	x4x4x8	x8x8	x16

Slot # 6 Occupied〔Mass Storage Controller〕	Disable Above 4G Decoding	Disables 64bit capable Device Resources to be Allocated in Above 4G Address Space.	
		Enabled	▶Disabled
	Disable PCIe Init	Disables BIOS built-in PCI Express Initialization for currently selected and down stream PCI Device(s).	
		Enabled	▶Disabled
	Disable PCIe GEN2	Disables BIOS built-in PCI Express GEN2 Initialization for currently selected and down stream PCI Device(s).	
		Enabled	▶Disabled
	PCI Express GEN 1-2 Settings	change PCI Express GEN 1-2 Settings of This Device.	
Slot # 7 Occupied〔Mass Storage Controller〕	Disable Above 4G Decoding	Disables 64bit capable Device Resources to be Allocated in Above 4G Address Space.	
		Enabled	▶Disabled
	Disable PCIe Init	Disables BIOS built-in PCI Express Initialization for currently selected and down stream PCI Device(s).	
		Enabled	▶Disabled
	Disable PCIe GEN 2	Disables BIOS built-in PCI Express GEN2 Initialization for currently selected and down stream PCI Device(s).	
		Enabled	▶Disabled
	PCI Express GEN 1-2 Settings	change PCI Express GEN 1-2 Settings of This Device.	

4.4.12 USB Configuration

USB Configuration Parameters.

USB Configuration					
Legacy USB Support	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.				
	Auto	▶Enabled	Disabled		
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.				
	▶Enabled	Disabled			
USB Mass Storage Driver Support	Enable/Disable USB Mass Storage Driver Support.				
	▶Enabled	Disabled			
Port 60/64 Emulation	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.				
	▶Enabled	Disabled			
USB transfer time-out	The time-out value for Control, Bulk, and Interrupt transfers.				
	1 sec	5 sec	10 sec	▶20 sec	
Device reset time-out	USB mass storage device Start Unit command time-out.				
	10 sec	▶20 sec	30 sec	40 sec	
Device power-up delay	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.				
	▶Auto	Manual			
AMI Virtual CDROM0 1.00	Mass storage device emulation type. 'AUTO' enumerates devices according to their media format. Optical drives are emulated as 'CDROM', drives with no media will be emulated according to a drive type.				
	▶Auto	Floppy	Forced FDD	Hard Disk	CD-ROM
AMI Virtual HDisk0 1.00	Mass storage device emulation type. 'AUTO' enumerates devices according to their media format. Optical drives are emulated as 'CDROM', drives with no media will be emulated according to a drive type.				
	▶Auto	Floppy	Forced FDD	Hard Disk	CD-ROM

4.4.13 Network Stack Configuration

Network Stack Settings.

Network Stack Configuration		
Network Stack	Enable/Disable UEFI Network Stack.	
	▶Enabled	Disabled
IPv4 PXE Support	Enables/disables IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.	
	▶Enabled	Disabled
IPv4 HTTP Support	Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.	
	Enabled	▶Disabled
IPv6 PXE Support	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.	
	Enabled	▶Disabled
IPv6 HTTP Support	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.	
	Enabled	▶Disabled
PXE boot wait time	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.	
	0	
Media detect count	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.	
	1	

4.4.14 NVMe Configuration

NVMe Device Options Settings.

4.4.15 AMD Mem Configuration Status

To display memory configuration (initialized by ABL) status.

AMD Mem Configuration Status		
Socket 0	Socket-specific memory configuration status.	
	Channel 0-11	Channel-specific memory configuration status.
Socket 1	Socket-specific memory configuration status.	
	Channel 0-11	Channel-specific memory configuration status.

4.4.16 Tls Auth Configuration

Press <Enter> to select Tls Auth Configuration.

T1s Auth Configuration				
Server CA Configuration	Press <Enter> to configure Server CA.			
	Enroll Cert	Enroll Cert Using File	Enroll Cert using file.	
		Cert GUID	Input digit character in 11111111-2222-3333-4444-1234567890ab format.	
		Commit Changes and Exit	Commit Changes and Exit.	
		Discard Changes and Exit	Discard Cchanges and Eexit.	
	Delete Cert	FE9C6606-8B49-44A3-8B6B-DEA3A0E0324D	GUID for CERT	
			Enabled	▶Disabled

4.4.17 RAM Disk Configuration

Press <Enter> to add/remove RAM disks.

RAM Disk Configuration		
Disk Memory Type	Specifies type of memory to use from available memory pool in system to create a disk.	
	►Boot Service Data	Reserved
Create raw	Size (Hex)	The valid RAM disk size should be multiples of the RAM disk block size.
		►1
	Create & Exit	Create a new RAM disk with the given starting and ending address.
	Discard & Exit	Discard and exits.
Create from file	Create a RAM disk from a given file.	
Remove selected RAM disk(s)	Removes selected RAM disk(s).	

4.4.18 AMD PBS

AMD PBS Setup Page.

AMD PBS				
RAS	RAS Periodic SMI Control	Enable/ disable Periodic SMI for polling [MCA Threshold] error.		
		►Enabled	Disabled	
	SMI Threshold	The [SMI Threshold] limits the number of [MCA Threshold and Deferred Error SMI source] per a Unit time (Defined by [SMI Scale]). (Default: 5 dec interrupts)		
		5		
	SMI Scale	The [SMI Scale] defines the time scale. (Default: 1000 dec)		
		1000		
	SMI Scale Unit	The [SMI Scale Unit] defines the unit of time scale. (Default: ms)		
		►millisecond	second	minute
	SMI Period	The [SMI Period] defines the polling interval (Default: 1000 dec, Maximum: 32767 dec, 0: Disable, Unit: ms)		
		1000		
	GHES Notify Type	Notification type for deferred/corrected errors.		
		►Polled	SCI	
	GHES UnCorr Notify Type	Notification type for uncorrected errors.		
		Polled	►NMI	
	PCIe GHES Notify Type	Notification type for PCIe corrected errors.		
		►Polled	SCI	
	PCIe UnCorr GHES Notify Type	Notification type for PCIe uncorrected errors.		
		Polled	►NMI	
	PCIe Root Port Corr Err Mask Reg	Initialize the PCIe AER Corrected Error Mask register of Root Port.		
		0		
	PCIe Root Port UnCorr Err Mask Reg	Initialize the PCIe AER Uncorrected Error Mask register of Root Port.		
		0		
	Pcie Root Port UnCorr Error Sev Reg	Initialize the PCIe AER Uncorrected Error Severity registers of Root Port.		
		7EF6030		
	PCIe Device Corr Err Mask Reg	Initialize the PCIe AER Corrected Error Mask register of PCIe Device.		
		0		
	PCIe Device UnCorr Err Mask Reg	Initialize the PCIe AER Uncorrected Error Mask register of PCIe Device.		
		100000		

RAS	Pcie Device UnCorr Error Sev Reg	Initialize the PCIe AER Uncorrected Error Severity registers of PCIe Device.
		7EF6030
	CXL DP CIE Mask Enable	Enable/Disable masking of CXL DP Correctable Error - Internal Error.
		▶Enabled | Disabled
	DRAM Hard Post Package Repair	This feature allows spare DRAM rows to replace malfunctioning rows via an in-field repair mechanism.
		Enabled | ▶Disabled
	HEST DMC Structure Support	HEST DMC(Deferred Machine Check) Structure Support.
		Enabled | ▶Disabled
	CXL Error Report Support	Enable/ disable CXL Error Reporting.
		Enabled | ▶Disabled
SPI Locking	Enable/ disable SPI Locking for protect ROM part.	
	Enabled | ▶Disabled	
HBA	Enable/Disable HBA for Standard backplane, Do not enable for Full Nvme backplane.	
	Enabled | ▶Disabled	
iLA TraceMemoryEn	Reserved 1M bytes MMIO space on 1M boundary when iLA TraceMemoryEn enabled.	
	Enabled | ▶Disabled	
CXL Range Encryption	Range 1-7 Memory Base	Enter memory range base address and limit address.
		0
	Range 1, 2, 4, 5 Memory Limit	Enter memory range base address and limit address.
		0
	Range 3, 6, 7 Memory Size	Enter memory range base address and limit address.
		0
	Start CXL Range Encryption	Start to encrypt all memory ranges.

4.4.19 Asmedia 106x Controller #0

Asmedia 106x Controller.

4.4.20 VLAN Configuration (MAC:020874FB2183)

VLAN Configuration.(MAC:020874FB2183)

VLAN Configuration		
Enter Configuration Menu	Press ENTER to enter configuration menu for VLAN configuration.	
	VLAN ID	VLAN ID of new VLAN or existing VLAN, valid value is 0~4094
		0
	Priority	802.1Q Priority, valid value is 0~7
		0
	Add VLAN	Create a new VLAN or update existing VLAN
		0
	Remove VLAN	Remove selected VLANs
		0

4.4.21 MAC:020874FB2183-IPv4 Network Configuration

Configure network parameters.(MAC:020874FB2183)

MAC:020874FB2183-IPv4 Network Configuration		
Configured	Indicate whether network address configured successfully or not.	
	Enabled	▶Disabled
Save Changes and Exit	Save Changes and Exit	

4.4.22 MAC:020874FB2183-IPv6 Network Configuration

Configure IPv6 network parameters.(MAC:020874FB2183)

MAC:020874FB2183-IPv6 Network Configuration			
Enter Configuration Menu	Press ENTER to enter configuration menu for IPv6 configuration.		
	Interface ID	The 64 bit alternative interface ID for the device. The string is colon separated. e.g. ff:dd:88:66:cc:1:2:3	
		0:8:74:FF:FE:FB:21:83	
	DAD Transmit Count	The number of consecutive Neighbor Solicitation messages sent while performing Duplicate Address Detection on a tentative address. A value of zero indicates that Duplicate Address Detection is not performed.	
		1	
	Policy	automatic or manual.	
		▶automatic	manual
	Save Changes and Exit	Save Changes for interface ID, DAD transmit count, policy, and data in advanced configuration.	

4.4.23 Broadcom BCM57416 NetXtreme-E 10GBASE-T RDMA Ethernet Controller-00:15:B2:B4:A4:0A

Configure Device Parameters.

Broadcom BCM57416 NetXtreme-E 10GBASE-T RDMA Ethernet Controller-00:15:B2:B4:A4:0A			
Firmware Image Menu	Family Firmware Version	Installed device firmware family version information.	
		227.1.114.0	
	Boot Code	Bootcode.	
		227.0.135.0	
	MBA	Multiple Boot Agent.	
		227.0.133.0	
	EFI	UEFI Option ROM.	
		227.0.133.0	
	NCSI	Management FW.	
		227.0.135.0	
	RDMA FW	RDMA FW.	
		227.0.135.0	
Device Configuration Menu	Multi-Function Mode	Configure NIC Hardware Mode. Switching from multi-function to single function will result in the clearing of Virtual Function values in the extended partitions. Advanced NPar option is a feature preview only.	
		▶SF	NPAR 1.0
	SR-IOV	Enable/Disable Single Root I/O Virtualization.	
		Enabled	▶Disabled
	Number of MSI-X Vectors per VF	Configure number of MSI-X Vectors per VF (1-64).	
		16	
	Maximum Number of PF MSI-X Vectors	Configure maximum number of PF MSI-X Vectors (0-512 per controller).	
		74	
	Energy Efficient Ethernet	Configure Energy Efficient Ethernet operation.	
		Enabled	▶Disabled
	Operational Link Speed	Configure the default link speed for the selected port. On dual port adapters, if one port is configured for 10G and user selects 25G on the other port, both ports will be set to 25G, or vice versa. If either port is set to Auto Negotiated, ensure that one port does not attempt to operate at 10 Gbps while the...	
		AutoNeg	
	Support RDMA	Configure RDMA Support for this port.	
		Enabled	▶Disabled

Device Configuration Menu	DCB Protocol	Enable/Disable DCB Protocol.			
		▶Disabled	Enabled (IEEE only)	CEE (only)	Both (IEEE preferred with fallback to CEE)
	LLDP nearest bridge	Configure LLDP nearest bridge state.			
		▶Enabled		Disabled	
	Default EVB Mode	Configure Default Edge Virtual Bridging mode.			
		▶VEB	VEPA	None	
	Enable PME Capability	Configure PME Capability support.			
		▶Enabled		Disabled	
	Flow Offload	Configure Flow Offload Mode. This feature is supported on Linux DPDK only. Not supported on Windows or ESX OS.			
		Enabled		▶Disabled	
	Adapter Error Recovery	Enable recovery of firmware from fatal errors without manual intervention, host reboot and power cycle.			
		Enabled		▶Disabled	
MBC Configuration Menu	Option ROM	Controls the enablement of legacy Boot Protocols in the Option ROM.			
		▶Enabled		Disabled	
	Legacy Boot Protocol	Select a boot protocol to be used in legacy BIOS (non-UEFI) boot mode.			
		▶PXE		NONE	
	Boot Strap Type	Specify the boot strap method used to boot to the operating system.			
		▶Auto Detect	BBS	Int 18h	Int 19h
	Pre-boot Wake On LAN	Configure Pre-boot Wake on LAN(WOL).			
		▶Enabled		Disabled	
	VLAN Mode	Virtual LAN mode enables use of a VLAN tag.			
		Enabled		▶Disabled	
	Boot Retry Count	Specify the number of retries to attempt in case of a boot failure.			
		No Retry	1 Retry	2 Retries	3 Retries
		4 Retries	▶5 Retries	6 Retries	Indefinite Retries
Blink LEDs	Blink LEDs for a duration up to 15 seconds.				
	0				
Link Status	Link Status.				
	Disconnected				
Permanent MAC Address	Permanent MAC Address.				
	00:15:B2:B4:A4:0A				
Virtual MAC Address	Virtual MAC Address.				
	00:15:B2:B4:A4:0A				
Restore Defaults	Reset adapter to factory defaults.				

4.4.24 VLAN Configuration (MAC:0015B2B4A40A)

VLAN Configuration (MAC:0015B2B4A40A)

VLAN Configuration (MAC:0015B2B4A40A)		
Enter Configuration Menu	Press ENTER to enter configuration menu for VLAN configuration.	
	VLAN ID	VLAN ID of new VLAN or existing VLAN, valid value is 0~4094.
		0
	Priority	802.1Q Priority, valid value is 0~7.
		0
	Add VLAN	Create a new VLAN or update existing VLAN.
	Remove VLAN	Remove selected VLANs

4.4.25 MAC:0015B2B4A40A-IPv4 Network Configuration

Configure network parameters. (MAC:0015B2B4A40A)

MAC:0015B2B4A40A-IPv4 Network Configuration		
Configured	Indicate whether network address configured successfully or not.	
	Enabled	▶Disabled
Save Changes and Exit	Save Changes and Exit.	

4.4.26 MAC:0015B2B4A40A-IPv6 Network Configuration

Configure IPv6 network parameters. (MAC:0015B2B4A40A)

MAC:0015B2B4A40A-IPv6 Network Configuration		
Enter Configuration Menu	Press ENTER to enter configuration menu for IPv6 configuration.	
	Interface ID	The 64 bit alternative interface ID for the device. The string is colon separated. e.g. ff:dd:88:66:cc:1:2:3
		2:15:B2:FF:FE:B4:A4:A
	DAD Transmit Count	The number of consecutive Neighbor Solicitation messages sent while performing Duplicate Address Detection on a tentative address. A value of zero indicates that Duplicate Address Detection is not performed.
		1
	Policy	automatic or manual.
		▶automatic | manual
	Save Changes and Exit	Save Changes for interface ID, DAD transmit count, policy, and data in advanced configuration.

4.4.27 Broadcom BCM57416 NetXtreme-E 10GBASE-T RDMA Ethernet Controller-00:15:B2:B4:A4:0B

Configure Device Parameters.

Broadcom BCM57416 NetXtreme-E 10GBASE-T RDMA Ethernet Controller-00:15:B2:B4:A4:0B		
Firmware Image Menu	Family Firmware Version	Installed device firmware family version information.
		227.1.114.0
	Boot Code	Bootcode.
		227.0.135.0
	MBA	Multiple Boot Agent.
		227.0.133.0
	EFI	UEFI Option ROM.
		227.0.133.0
	NCSI	Management FW.
		227.0.135.0
	RDMA FW	RDMA FW.
		227.0.135.0
Device Configuration Menu	Multi-Function Mode	Configure NIC Hardware Mode. Switching from multi-function to single function will result in the clearing of Virtual Function values in the extended partitions. Advanced NPar option is a feature preview only.
		▶SF | NPAR 1.0
	SR-IOV	Enable/Disable Single Root I/O Virtualization.
		Enabled | ▶Disabled
	Number of MSI-X Vectors per VF	Configure number of MSI-X Vectors per VF (1-64).
		16
	Maximum Number of PF MSI-X Vectors	Configure maximum number of PF MSI-X Vectors (0-512 per controller).
		74
	Energy Efficient Ethernet	Configure Energy Efficient Ethernet operation.
		Enabled | ▶Disabled
	Operational Link Speed	Configure the default link speed for the selected port. On dual port adapters, if one port is configured for 10G and user selects 25G on the other port, both ports will be set to 25G, or vice versa. If either port is set to Auto Negotiated, ensure that one port does not attempt to operate at 10 Gbps while the...
		AutoNeg

Device Configuration Menu	Support RDMA	Configure RDMA Support for this port.			
		Enabled		▶Disabled	
	DCB Protocol	Enable/Disable DCB Protocol.			
		▶Disabled	Enabled (IEEE only)	CEE (only)	Both (IEEE preferred with fallback to CEE)
	LLDP nearest bridge	Configure LLDP nearest bridge state.			
		▶Enabled		Disabled	
	Default EVB Mode	Configure Default Edge Virtual Bridging mode.			
		▶VEB	VEPA	None	
	Enable PME Capability	Configure PME Capability support.			
		▶Enabled		Disabled	
	Flow Offload	Configure Flow Offload Mode. This feature is supported on Linux DPDK only. Not supported on Windows or ESX OS.			
		Enabled		▶Disabled	
	Adapter Error Recovery	Enable recovery of firmware from fatal errors without manual intervention, host reboot and power cycle.			
		Enabled		▶Disabled	
MBC Configuration Menu	Option ROM	Controls the enablement of legacy Boot Protocols in the Option ROM.			
		▶Enabled		Disabled	
	Legacy Boot Protocol	Select a boot protocol to be used in legacy BIOS (non-UEFI) boot mode.			
		▶PXE		NONE	
	Boot Strap Type	Specify the boot strap method used to boot to the operating system.			
		▶Auto Detect	BBS	Int 18h	Int 19h
	Pre-boot Wake On LAN	Configure Pre-boot Wake on LAN(WOL).			
		▶Enabled		Disabled	
	VLAN Mode	Virtual LAN mode enables use of a VLAN tag.			
		Enabled		▶Disabled	
	Boot Retry Count	Specify the number of retries to attempt in case of a boot failure.			
		No Retry	1 Retry	2 Retries	3 Retries
		4 Retries	▶5 Retries	6 Retries	Indefinite Retries
Blink LEDs	Blink LEDs for a duration up to 15 seconds.				
	0				
Link Status	Link Status.				
	Disconnected				
Permanent MAC Address	Permanent MAC Address.				
	00:15:B2:B4:A4:0B				
Virtual MAC Address	Virtual MAC Address.				
	00:15:B2:B4:A4:0B				
Restore Defaults	Reset adapter to factory defaults.				

4.4.28 VLAN Configuration (MAC:0015B2B4A40B)

VLAN Configuration (MAC:0015B2B4A40B)

VLAN Configuration (MAC:0015B2B4A40B)		
Enter Configuration Menu	Press ENTER to enter configuration menu for VLAN configuration.	
	VLAN ID	VLAN ID of new VLAN or existing VLAN, valid value is 0~4094.
		0
	Priority	802.1Q Priority, valid value is 0~7.
		0
	Add VLAN	Create a new VLAN or update existing VLAN.
	Remove VLAN	Remove selected VLANs

4.4.29 MAC:0015B2B4A40B-IPv4 Network Configuration

Configure network parameters. (MAC:0015B2B4A40B)

MAC:0015B2B4A40B-IPv4 Network Configuration			
Configured	Indicate whether network address configured successfully or not.		
	Enabled	▶Disabled	
Save Changes and Exit	Save Changes and Exit.		

4.4.30 MAC:0015B2B4A40B-IPv6 Network Configuration

Configure IPv6 network parameters. (MAC:0015B2B4A40B)

MAC:0015B2B4A40B-IPv6 Network Configuration			
Enter Configuration Menu	Press ENTER to enter configuration menu for IPv6 configuration.		
	Interface ID	The 64 bit alternative interface ID for the device. The string is colon separated. e.g. ff:dd:88:66:cc:1:2:3	
		2:15:B2:FF:FE:B4:A4:B	
	DAD Transmit Count	The number of consecutive Neighbor Solicitation messages sent while performing Duplicate Address Detection on a tentative address. A value of zero indicates that Duplicate Address Detection is not performed.	
		1	
	Policy	automatic or manual.	
		▶automatic	manual
	Save Changes and Exit	Save Changes for interface ID, DAD transmit count, policy, and data in advanced configuration.	

4.4.31 Inter(R) I210 Gigabit Nerwork Connection-00:15:B2:B4:A4:0C

Configure Gigabit Ethernet device parameters.

Inter(R) I210 Gigabit Nerwork Connection-00:15:B2:B4:A4:0C						
NIC Configuration	Click to configure the network device port.					
	Link Speed	Specifies the port speed used for the selected boot protocol.				
		▶Auto Negotiated	10 Mbps Half	10 Mbps Full	100 Mbps Half	100 Mbps Full
	Wake On LAN	Enables power on of the system via LAN. Note that configuring Wake on LAN in the operating system does not change the value of this setting, but does override the behavior of Wake on LAN in OS controlled power states.				
		▶Enabled	Disabled			
Blink LEDs	Blink LEDs for a duration up to 15 seconds.					
	0					

4.4.32 VLAN Configuration (MAC:0015B2B4A40C)

VLAN Configuration (MAC:0015B2B4A40C)

VLAN Configuration (MAC:0015B2B4A40B)		
Enter Configuration Menu	Press ENTER to enter configuration menu for VLAN configuration.	
	VLAN ID	VLAN ID of new VLAN or existing VLAN, valid value is 0~4094.
		0
	Priority	802.1Q Priority, valid value is 0~7.
		0
	Add VLAN	Create a new VLAN or update existing VLAN.
	Remove VLAN	Remove selected VLANs

4.4.33 MAC:0015B2B4A40C-IPv4 Network Configuration

Configure network parameters. (MAC:0015B2B4A40C)

MAC:0015B2B4A40C-IPv4 Network Configuration		
Configured	Indicate whether network address configured successfully or not.	
	Enabled	▶Disabled
Save Changes and Exit	Save Changes and Exit.	

4.4.34 MAC:0015B2B4A40C-IPv6 Network Configuration

Configure IPv6 network parameters. (MAC:0015B2B4A40C)

MAC:0015B2B4A40C-IPv6 Network Configuration			
Enter Configuration Menu	Press ENTER to enter configuration menu for IPv6 configuration.		
	Interface ID	The 64 bit alternative interface ID for the device. The string is colon separated. e.g. ff:dd:88:66:cc:1:2:3	
		2:15:B2:FF:FE:B4:A4:C	
	DAD Transmit Count	The number of consecutive Neighbor Solicitation messages sent while performing Duplicate Address Detection on a tentative address. A value of zero indicates that Duplicate Address Detection is not performed.	
		1	
	Policy	automatic or manual.	
		▶automatic	manual
	Save Changes and Exit	Save Changes for interface ID, DAD transmit count, policy, and data in advanced configuration.	

4.4.35 Driver Health

Provides Health Status for the Drivers/Controllers.

Driver Health		
Intel (R) PRO/1000 8.7.10 PCI-E	Provides Health Status for the Drivers/Controllers.	
	Healthy	
	Controller 59151018 Child 0	Provides Health Status for the Drivers/Controllers.
		Healthy
	Intel (R) I210 Gigabit Network Connection	Provides Health Status for the Drivers/Controllers.
		Healthy
Broadcom NXE Gigabit Ethernet Driver	Provides Health Status for the Drivers/Controllers.	
	Healthy	
	Controller 592E3F98 Child 0	Provides Health Status for the Drivers/Controllers.
		Healthy
	Controller 592E3F98 Child 58842618	Provides Health Status for the Drivers/Controllers.
		Healthy
Broadcom NXE Gigabit Ethernet Driver	Provides Health Status for the Drivers/Controllers.	
	Healthy	
	Controller 592E5818 Child 0	Provides Health Status for the Drivers/Controllers.
		Healthy
	Controller 592E5818 Child 5852DE18	Provides Health Status for the Drivers/Controllers.
		Healthy

4.5 Chipset



4.5.1 PCIe Compliance Mode

PCIe Link Compliance Mode.

On
▶Off

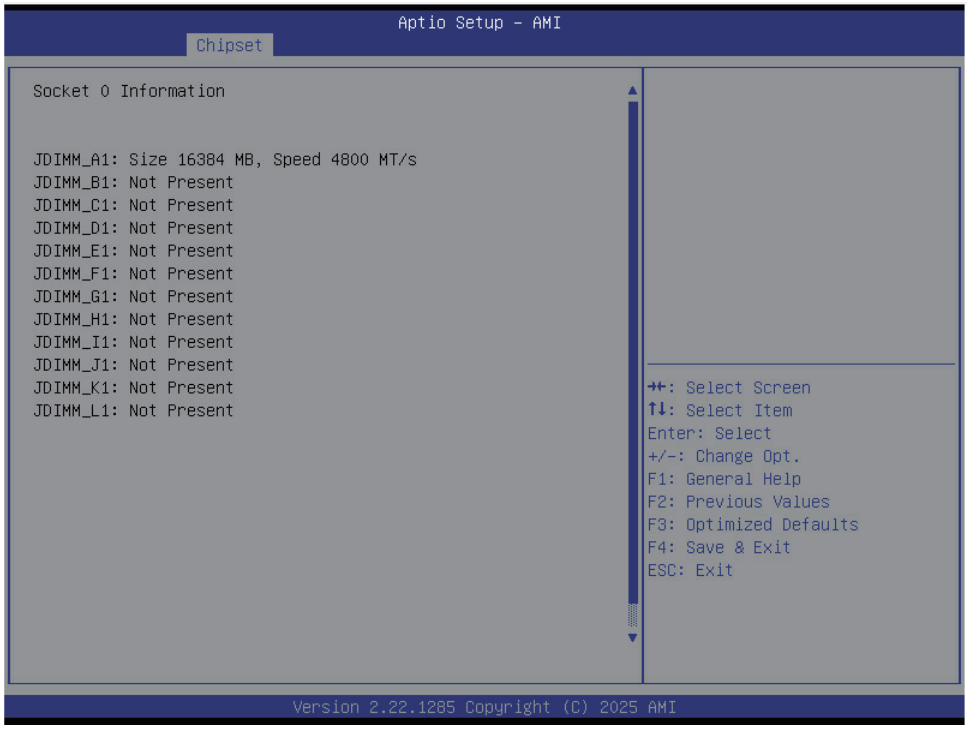
4.5.2 South Bridge

South Bridge Parameters

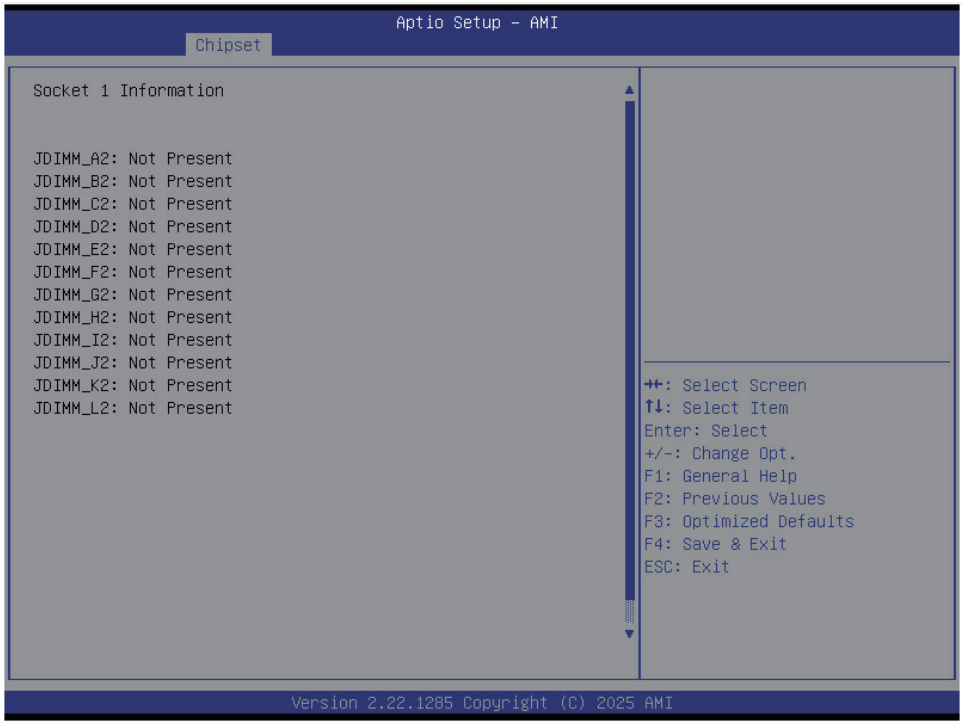
South Bridge				
SB Debug Configuration	Options For SB Debug Features.			
	SB SATA DEBUG Configuration	Aggressive Link PM Capability	Indicates Whether Host Bus Adapter (HBA) Can Support Auto-Generating Link Requests To The Partial Or Slumber States When There Are No Commands To Process.	
			►Enable	Disable
		Port Multiplier Capability	Indicates Whether Host Bus Adapter (HBA) Can Support A Port Multiplier.	
			►Enable	Disable
		SATA Ports Auto Clock Control	Enable/disable SATA Ports Auto Clock Control.	
			►Enable	Disable
		SATA Partial State Capability	Indicates Whether SATA Host Bus Adapter (HBA) Can Support Transitions To The Partial State.	
			►Enable	Disable
		SATA FIS Based Switching	Indicates Whether SATA Host Bus Adapter (HBA) Can Support Port Multiplier FIS-Based Switching.	
			►Enable	Disable
		SATA Command Completion Coalescing Support	Indicates Whether SATA Host Bus Adapter (HBA) Can Support Command Completion Coalescing.	
			Enable	►Disable
		SATA Slumber State Capability	Indicates Whether SATA Host Bus Adapter (HBA) Can Support Transitions To The Slumber State.	
			►Enable	Disable
		SATA Target Support 8 Devices	Indicates Whether SATA Target Support 8 Devices Function.	
			Enable	►Disable
		Generic Mode	Sata Disable Generic Mode.	
			Enable	►Disable
		SATA AHCI Enclosure	SATA AHCI Enclosure Management.	
			Enable	►Disable
		SATA SGPIO 0	Enable/Disable SATA Serial General Purpose Input/Output (SGPIO) 0.	
			Enable	►Disable
	SB FUSION DEBUG Configuration	TimerTick Tracking	Enable	►Disable
		Clock Interrupt Tag	Enable	►Disable
	SB MISC DEBUG Configuration	SB Clock Spread Spectrum	Enable/Disable CG1_PLL Spread Spectrum.	
			Enable	►Disable
		HPET In SB	HPET Function Switch	
			►Enable	Disable
		MsiDis in HPET	Expose MSI capability in HPET Capbility register.	
			►Enable	Disable

4.5.3 North Bridge
North Bridge Parameters

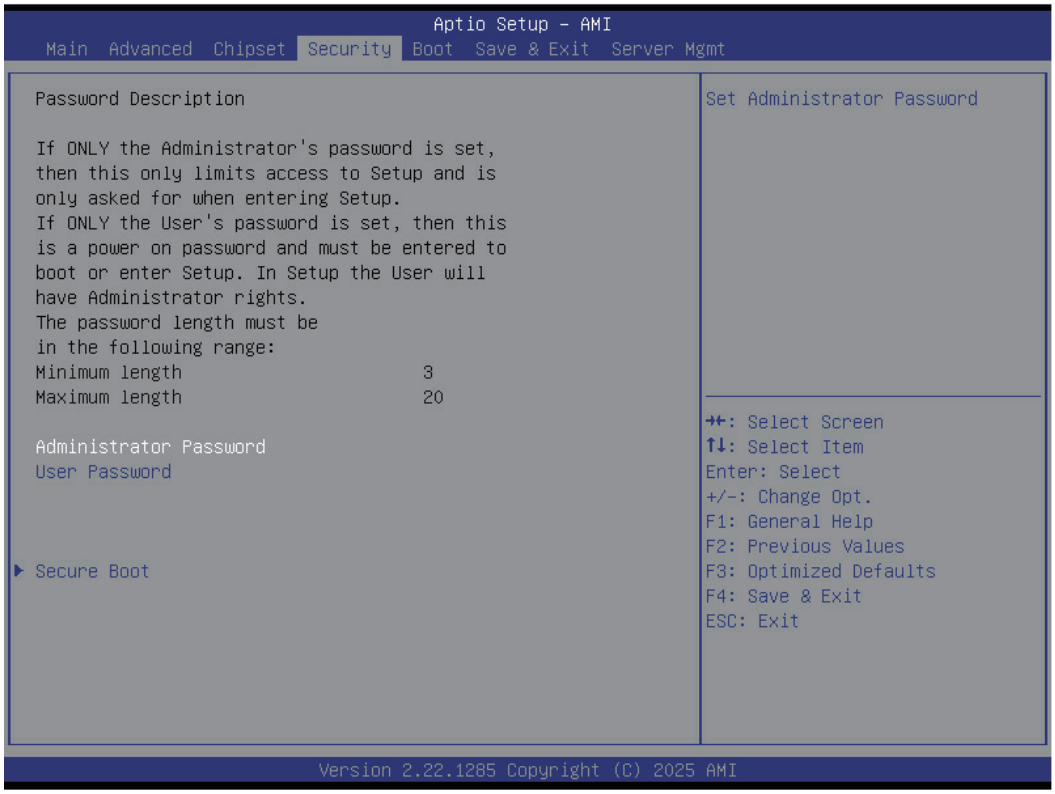
Socket 0 Information
Example for installing one DIMM, please refer to the screenshot below.



Socket 1 Information
Example for installing one DIMM, please refer to the screenshot below.

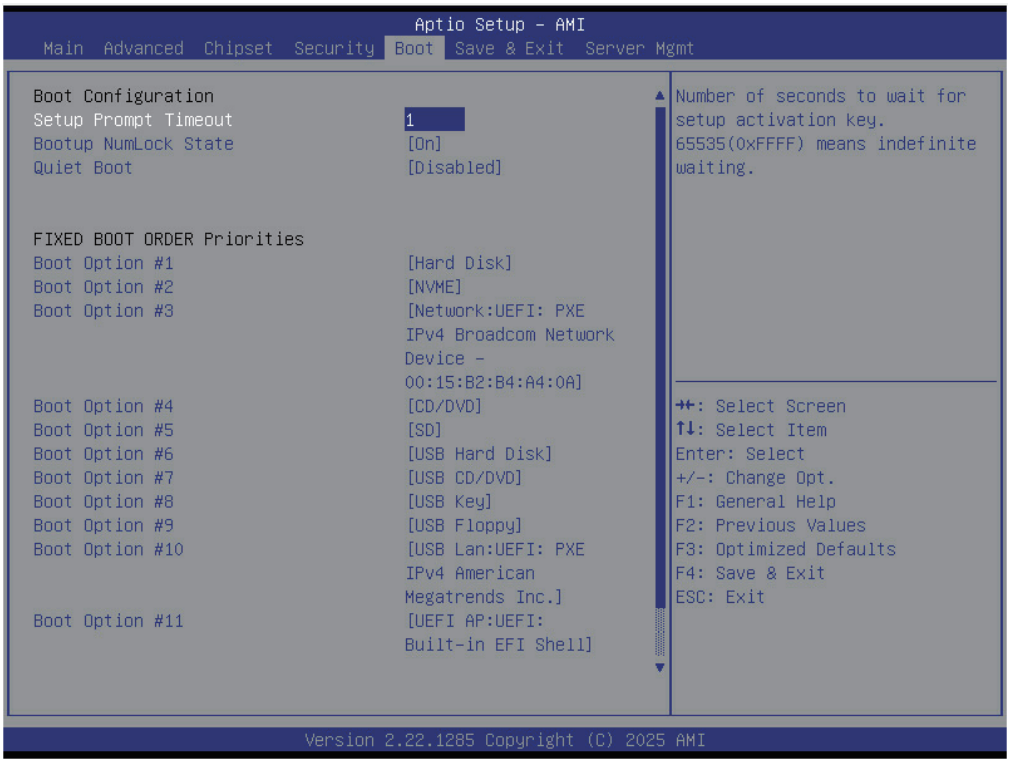


4.6 Security



Security			
Administrator Password	Set Administrator password.		
User Password	Set User password.		
Secure Boot	Secure Boot	Secure Boot feature is Active if Secure Boot is Enabled, Platform Key(PK) is enrolled and the System is in User mode. The mode change requires platform reset.	
		▶Enabled	Disabled
	Secure Boot Mode	Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.	
		▶Standard	Custom

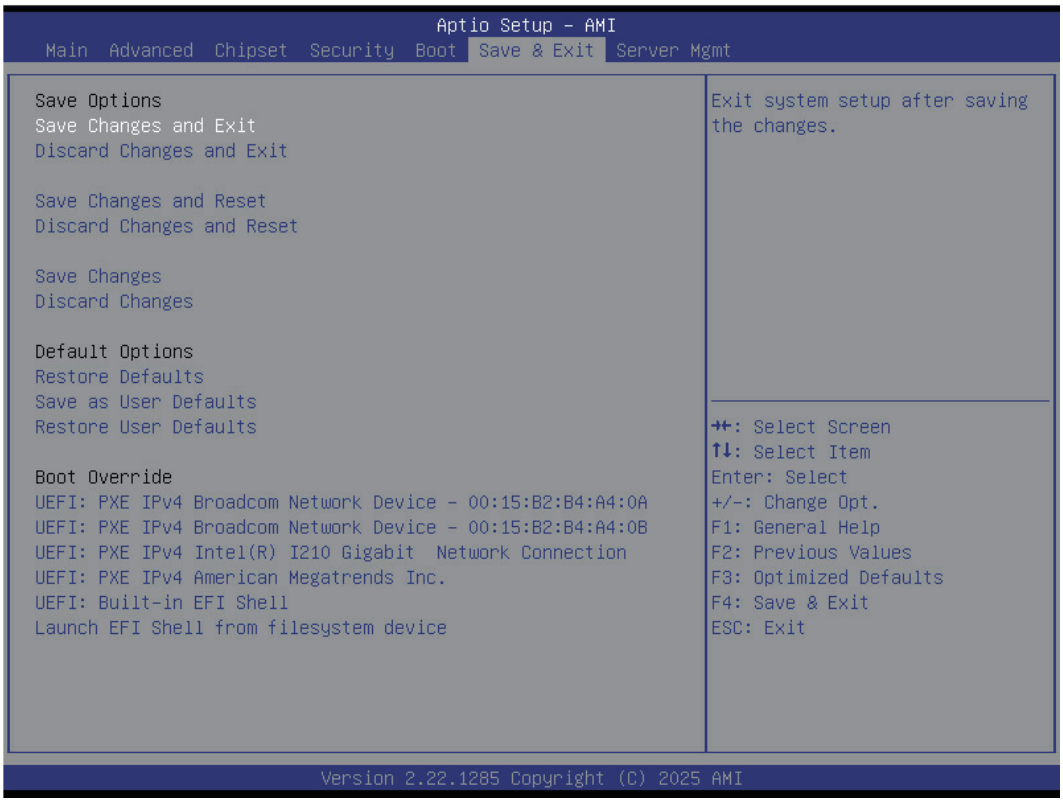
4.7 Boot



Boot				
Set Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.			
	1			
Bootup Numlock State	Select the keyboard Numlock state.			
	▶On		Off	
Quiet Boot	Enables/disables Quiet Boot option.			
	Enable		▶Disabled	
Boot Option #1	Sets the system boot order.			
	▶Hard Disk	NVME	Network:UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A	CD/DVD
	SD	USB Hard Disk	USB CD/DVD	USB Key
	USB Floppy	USB Lan:UEFI:PXE IPv4 American Megatrends Inc.	UEFI AP:UEFI:Built-in EFI Shell	Disabled
Boot Option #2	Sets the system boot order.			
	Hard Disk	▶NVME	Network:UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A	CD/DVD
	SD	USB Hard Disk	USB CD/DVD	USB Key
	USB Floppy	USB Lan:UEFI:PXE IPv4 American Megatrends Inc.	UEFI AP:UEFI:Built-in EFI Shell	Disabled
Boot Option #3	Sets the system boot order.			
	Hard Disk	NVME	▶Network:UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A	CD/DVD
	SD	USB Hard Disk	USB CD/DVD	USB Key
	USB Floppy	USB Lan:UEFI:PXE IPv4 American Megatrends Inc.	UEFI AP:UEFI:Built-in EFI Shell	Disabled
Boot Option #4	Sets the system boot order.			
	Hard Disk	NVME	Network:UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A	▶CD/DVD
	SD	USB Hard Disk	USB CD/DVD	USB Key
	USB Floppy	USB Lan:UEFI:PXE IPv4 American Megatrends Inc	UEFI AP:UEFI:Built-in EFI Shell	Disabled

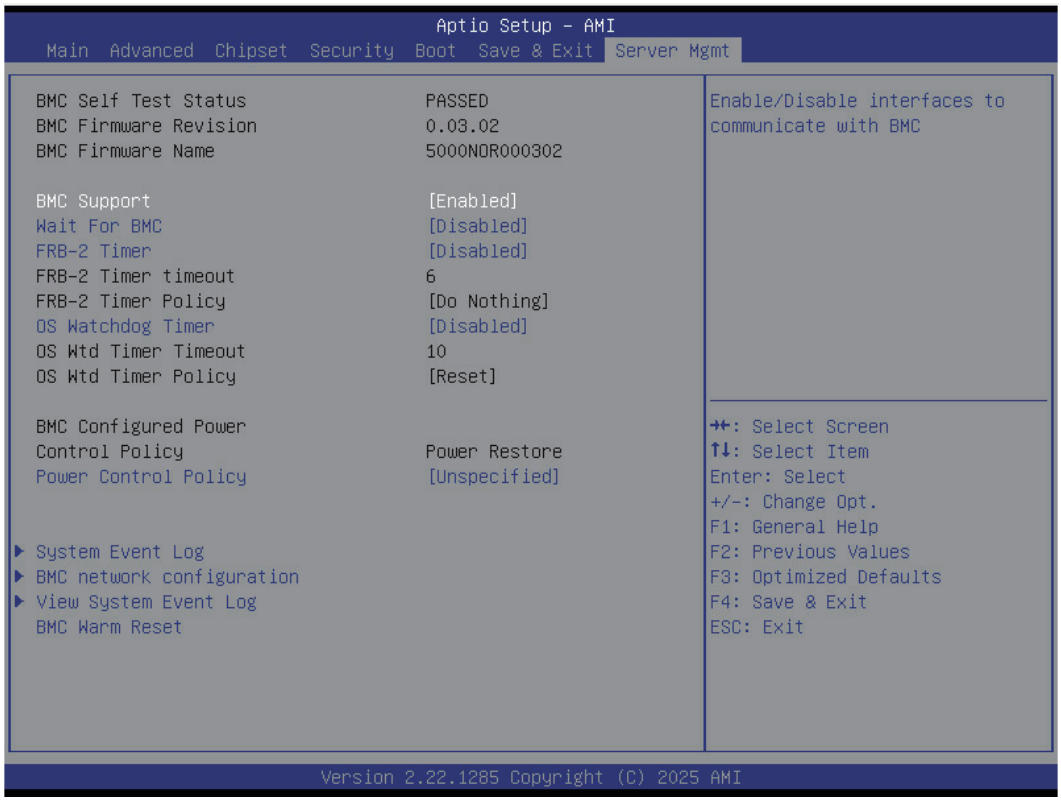
<table>
<tr><td rowspan="4">Boot Option #5</td><td colspan="4">Sets the system boot order.</td></tr>
<tr><td>Hard Disk</td><td>NVME</td><td>Network:UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A</td><td>CD/DVD</td></tr>
<tr><td>►SD</td><td>USB Hard Disk</td><td>USB CD/DVD</td><td>USB Key</td></tr>
<tr><td>USB Floppy</td><td>USB Lan:UEFI:PXE IPv4 American Megatrends Inc.</td><td>UEFI AP:UEFI:Built-in EFI Shell</td><td>Disabled</td></tr>
<tr><td rowspan="4">Boot Option #6</td><td colspan="4">Sets the system boot order.</td></tr>
<tr><td>Hard Disk</td><td>NVME</td><td>Network:UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A</td><td>CD/DVD</td></tr>
<tr><td>SD</td><td>►USB Hard Disk</td><td>USB CD/DVD</td><td>USB Key</td></tr>
<tr><td>USB Floppy</td><td>USB Lan:UEFI:PXE IPv4 American Megatrends Inc.</td><td>UEFI AP:UEFI:Built-in EFI Shell</td><td>Disabled</td></tr>
<tr><td rowspan="4">Boot Option #7</td><td colspan="4">Sets the system boot order.</td></tr>
<tr><td>Hard Disk</td><td>NVME</td><td>Network:UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A</td><td>CD/DVD</td></tr>
<tr><td>SD</td><td>USB Hard Disk</td><td>►USB CD/DVD</td><td>USB Key</td></tr>
<tr><td>USB Floppy</td><td>USB Lan:UEFI:PXE IPv4 American Megatrends Inc.</td><td>UEFI AP:UEFI:Built-in EFI Shell</td><td>Disabled</td></tr>
<tr><td rowspan="4">Boot Option #8</td><td colspan="4">Sets the system boot order.</td></tr>
<tr><td>Hard Disk</td><td>NVME</td><td>Network:UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A</td><td>CD/DVD</td></tr>
<tr><td>SD</td><td>USB Hard Disk</td><td>USB CD/DVD</td><td>►USB Key</td></tr>
<tr><td>USB Floppy</td><td>USB Lan:UEFI:PXE IPv4 American Megatrends Inc.</td><td>UEFI AP:UEFI:Built-in EFI Shell</td><td>Disabled</td></tr>
<tr><td rowspan="4">Boot Option #9</td><td colspan="4">Sets the system boot order.</td></tr>
<tr><td>Hard Disk</td><td>NVME</td><td>Network:UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A</td><td>CD/DVD</td></tr>
<tr><td>SD</td><td>USB Hard Disk</td><td>USB CD/DVD</td><td>USB Key</td></tr>
<tr><td>►USB Floppy</td><td>USB Lan:UEFI:PXE IPv4 American Megatrends Inc.</td><td>UEFI AP:UEFI:Built-in EFI Shell</td><td>Disabled</td></tr>
<tr><td rowspan="4">Boot Option #10</td><td colspan="4">Sets the system boot order.</td></tr>
<tr><td>Hard Disk</td><td>NVME</td><td>Network:UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A</td><td>CD/DVD</td></tr>
<tr><td>SD</td><td>USB Hard Disk</td><td>USB CD/DVD</td><td>USB Key</td></tr>
<tr><td>USB Floppy</td><td>►USB Lan:UEFI:PXE IPv4 American Megatrends Inc.</td><td>UEFI AP:UEFI:Built-in EFI Shell</td><td>Disabled</td></tr>
<tr><td rowspan="4">Boot Option #11</td><td colspan="4">Sets the system boot order.</td></tr>
<tr><td>Hard Disk</td><td>NVME</td><td>Network:UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A</td><td>CD/DVD</td></tr>
<tr><td>SD</td><td>USB Hard Disk</td><td>USB CD/DVD</td><td>USB Key</td></tr>
<tr><td>USB Floppy</td><td>USB Lan:UEFI:PXE IPv4 American Megatrends Inc.</td><td>►UEFI AP:UEFI:Built-in EFI Shell</td><td>Disabled</td></tr>
<tr><td rowspan="7">UEFI NETWORK Drive BBS Priorities</td><td colspan="4">Specifies the Boot Device Priority sequence from available UEFI NETWORK Drives.</td></tr>
<tr><td rowspan="3">Boot Option #1</td><td colspan="3">Sets the system boot order.</td></tr>
<tr><td>►UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A</td><td>UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0B</td></tr>
<tr><td>UEFI:PXE IPv4 Intel(R) I210 Gigabit Network Connection</td><td>Disable</td></tr>
<tr><td rowspan="3">Boot Option #2</td><td colspan="3">Sets the system boot order.</td></tr>
<tr><td>UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A</td><td>►UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0B</td></tr>
<tr><td>UEFI:PXE IPv4 Intel(R) I210 Gigabit Network Connection</td><td>Disable</td></tr>
<tr><td rowspan="3">Boot Option #3</td><td colspan="3">Sets the system boot order.</td></tr>
<tr><td>UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A</td><td>UEFI:PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0B</td></tr>
<tr><td>►UEFI:PXE IPv4 Intel(R) I210 Gigabit Network Connection</td><td>Disable</td></tr>
<tr><td rowspan="3">UEFI USB Lan Drive BBS Priorities</td><td colspan="4">Sets the system boot order.</td></tr>
<tr><td rowspan="2">Boot Option #1</td><td colspan="3">Sets the system boot order.</td></tr>
<tr><td>►UEFI:PXE IPv4 American Megatrends Inc.</td><td>Disable</td></tr>
<tr><td rowspan="3">UEFI Application Boot Priorities</td><td colspan="4">Specifies the Boot Device Priority sequence from available UEFI Application.</td></tr>
<tr><td rowspan="2">Boot Option #1</td><td colspan="3">Sets the system boot order.</td></tr>
<tr><td>►UEFI: Built-in EFI Shell</td><td>Disable</td></tr>
</table>

4.8 Save & Exit



Save & Exit	
Save Changes and Exit	Exit system setup after saving the changes.
Discard Changes and Exit	Exit system setup without saving any changes.
Save Changes and Reset	Reset the system after saving the changes.
Discard Changes and Reset	Reset system setup without saving any changes.
Save Changes	Save changes done so far to any of the setup options.
Discard Changes	Discard changes done so far to any of the setup options
Restore Defaults	Restore/Load default values for all the setup options.
Save as User Defaults	Save the changes done so far as user defaults.
Restore User Defaults	Restore the user Defaults to all the setup options.
UEFI: PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0A	
UEFI: PXE IPv4 Broadcom Network Device-00:15:B2:B4:A4:0B	
UEFI: PXE IPv4 Intel (R) I210 Gigabit Network Connection	
UEFI: PXE IPv4 American Megatrends Inc.	
UEFI: Built-in EFI Shell	
Launch EFI Shell from filesystem device	Attempts to Launch EFI Shell application (Shell.efi) from one of the available filesystem devices.

4.9 Server Mgmt



4.9.1 BMC Support

Enable/Disable interfaces to communicate with BMC.

▶Enabled
Disabled

4.9.2 Wait for BMC

Wait For BMC response for specified time out. In PILOTII, BMC starts at the same time when BIOS starts during AC power ON. It takes around 30 seconds to initialize Host to BMC interfaces.

Enabled
▶Disabled

4.9.3 FRB-2 Timer

Enable or Disable FRB-2 timer (POST timer).

Enabled
▶Disabled

4.9.4 OS Watchdog Timer timeout

Enter value Between 1 to 30 min for FRB-2 Timer Expiration.

Enabled
▶Disabled

4.9.5 Power Control Policy

Configure how the system should respond if AC Power is lost,Reset not required as selected Power policy will be set in BMC when policy is saved.

Do Not PowerUp	Last Power State
Power Restore	▶Unspecified

4.9.6 System Event Log

Press <Enter> to change the SEL event log configuration.

System Event Log				
SEL Components	Change this to enable or disable event logging for error/progress codes during boot.			
	▶Enabled	Disabled		
Erase SEL	Choose options for erasing SEL.			
	▶No	Yes, On next reset	Yes, On every reset	
When SEL is Full	Choose options for reactions to a full SEL.			
	▶Do Nothing	Erase Immediately	Delete Oldest Record	
Log EFI Status Codes	Disable the logging of EFI Status Codes or log only error code or only progress code or both.			
	Disabled	Both	▶Error code	Progress code

4.9.7 BMC network configurtion

Configure BMC network parameters.

BMC network configuration				
Lan channel 1				
Configuration Address source	Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.			
	▶Unspecified	Static	DynamicBmcDhcp	DynamicBmcNonDhcp
IPv6 Support	Enable/Disable LAN1 IPv6 Support.			
	▶Enabled	Disabled		
Configuration Address source	Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.			
	▶Unspecified	Static	DynamicBmcDhcp	
Configuration Gateway Lan1 Address source	Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.			
	▶Unspecified	Static	DynamicBmcDhcp	
VLAN Support	Enable VLAN Support to specify the 802.1q VLAN ID.			
	▶Unspecified	Enabled	Disabled	
Lan channel 2				
Configuration Address source	Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.			
	▶Unspecified	Static	DynamicBmcDhcp	DynamicBmcNonDhcp
IPv6 Support	Enable/Disable LAN2 IPv6 Support.			
	▶Enabled	Disabled		
Configuration Address source	Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.			
	▶Unspecified	Static	DynamicBmcDhcp	
Configuration Gateway Lan2 Address source	Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.			
	▶Unspecified	Static	DynamicBmcDhcp	
VLAN Support	Enable VLAN Support to specify the 802.1q VLAN ID.			
	▶Unspecified	Enabled	Disabled	

4.9.8 View System Event Log

Press <Enter> to view the System Event Log Records.

4.9.9 BMC Warm Reset

Press <Enter> to do Warm Reset BMC.

4.10 BIOS Post Code

There are two ways to get post code,
1. check the LED debug card
2. execute the IPMI command as below

(1) Read the first 256 bytes:$ipmitool -I lanplus -H "$BMC_IP" -U "$BMC_USER" -P "$BMC_PASSWD" raw 0x32 0x73 0x00
(2) Read the next 256 bytes: $ipmitool -I lanplus -H "$BMC_IP" -U "$BMC_USER" -P "$BMC_PASSWD" raw 0x32 0x73 0x02

NOTE
BMC IP: -H $BMC_IP
User Account: -U $BMC_USER
Password: -P $BMC_PASSWD

AMD PSP FW POST code
(FW output 2 bytes post code,but user only can see low byte on IPMI command output)

Post Code	Description
Start Processor Test Points	
0xE000	Entry used for range testing for @b Processor related TPs
Memory test points	
0xE001	Memory structure initialization (Public interface)
0xE002	SPD Data processing (Public interface)
0xE003	Memory configuration (Public interface) Phase 1
0xE004	DRAM initialization
0xE005	ProcMemSPDChecking
0xE006	ProcMemModeChecking
0xE007	Speed and TCL configuration
0xE008	ProcMemSpdTiming
0xE009	ProcMemDramMapping
0xE00A	ProcMemPlatformSpecificConfig
0xE00B	ProcMemPhyCompensation
0xE00C	ProcMemStartDcts
0xE00D	ProcMemBeforeDramInit (Public interface)
0xE00E	ProcMemPhyFenceTraining
0xE00F	ProcMemSynchronizeDcts
0xE010	ProcMemSystemMemoryMapping
0xE011	ProcMemMtrrConfiguration
0xE012	ProcMemDramTraining
0xE013	ProcMemBeforeAnyTraining(Public interface)
0xE014	ABL Mem - PMU - Before PMU Firmware load
0xE015	ABL Mem - PMU - After PMU Firmware load
0xE016	ABL Mem - PMU Populate SRAM Timing
0xE017	ABL Mem - PMU Populate SRAM Config
0xE018	ABL Mem - PMU Write SRAM Msg Block
0xE019	ABL Mem - Wait for Phy Cal Complete
0xE01A	ABL Mem - Phy Cal Complete
0xE01B	ABL Mem - PMU Start
0xE01C	ABL Mem - PMU Started

0xE01D	ABL Mem - PMU Waiting for Complete
0xE01E	ABL Mem - PMU Stage Dec Init
0xE01F	ABL Mem - PMU Stage Training Wr Lvl
0xE020	ABL Mem - PMU Stage Training Rx En
0xE021	ABL Mem - PMU Stage Training Rd Dqs
0xE022	ABL Mem - PMU Stage Traning Rd 2D
0xE023	ABL Mem - PMU Stage Training Wr 2D
0xE024	ABL Mem - PMU Queue Empty
0xE025	ABL Mem - PMU US message Start
0xE026	ABL Mem - PMU US message End
0xE027	ABL Mem - PMU Complete
0xE028	ABL Mem - PMU - After PMU Training
0xE029	ABL Mem - PMU - Before Disable PMU
0xE02A	ABL Mem - ProcMemTransmitDqsTraining
0xE02B	ABL Mem - Start write sweep
0xE02C	ABL Mem - Set Transmit DQ delay
0xE02D	ABL Mem - Write test pattern
0xE02E	ABL Mem - Read Test pattern
0xE02F	ABL Mem - Compare Test pattern
0xE030	ABL Mem - Update results
0xE031	ABL Mem - Start Find passing window
0xE032	ABL Mem - ProcMemMaxRdLatencyTraining
0xE033	ABL Mem - Start sweep
0xE034	ABL Mem - Set delay
0xE035	ABL Mem - Write test pattern
0xE036	ABL Mem - Read Test pattern
0xE037	ABL Mem - Compare Test pattern
0xE038	ABL Mem - Online Spare init
0xE039	ABL Mem - Chip select Interleave Init
0xE03A	ABL Mem - Node Interleave Init
0xE03B	ABL Mem - Channel Interleave Init
0xE03C	ABL Mem - ECC initialization
0xE03D	ABL Mem - Platform Specific Init
0xE03E	ABL Mem - Before callout for "AgesaReadSpd"
0xE03F	ABL Mem - After callout for "AgesaReadSpd"
0xE040	ABL Mem - Before optional callout "AgesaHookBeforeDramInit"
0xE041	ABL Mem - After optional callout "AgesaHookBeforeDramInit"
0xE042	ABL Mem - Before optional callout "AgesaHookBeforeDQSTraining"
0xE043	ABL Mem - After optional callout "AgesaHookBeforeDQSTraining"
0xE044	ABL Mem - Before optional callout "AgesaHookBeforeDramInit"
0xE045	ABL Mem - After optional callout "AgesaHookBeforeDramInit"
0xE046	ABL Mem - After MemDataInit
0xE047	ABL Mem - Before InitializeMCT
0xE048	ABL Mem - Before LV DDR3
0xE049	ABL Mem - Before InitMCT
0xE04A	ABL Mem - Before OtherTiming
0xE04B	ABL Mem - Before UMAMemTyping
0xE04C	ABL Mem - Before SetDqsEccTmgs

0xE04D	ABL Mem - Before MemClr
0xE04E	ABL Mem - Before On DIMM Thermal
0xE04F	ABL Mem - Before DMI
0xE050	ABL MEM - End of phase 3 memory code
0xE051	Entry point CPU init after training
0xE052	Exit point CPU init after training
0xE053	Entry point CPU APOB data init
0xE054	Exit point CPU APOB data init
0xE055	Entry point CPU Optimized boot init
0xE056	Exit point CPU Optimized boot init
0xE057	Entry point CPU APOB EDC info init
0xE058	Exit point CPU APOB EDC info init
0xE059	Entry point CPU APOB CCD map data init
0xE05A	Exit point CPU APOB CCD map data init
0xE080	ProcMemSendMRS2
0xE081	Sedding MRS3
0xE082	Sending MRS1
0xE083	Sending MRS0
0xE084	Continuous Pattern Read
0xE085	Continuous Pattern Write
0xE086	Mem: 2d RdDqs Training begin
0xE087	Mem: Before optional callout to platform BIOS to change External Vref during 2d Training
0xE088	Mem: After optional callout to platform BIOS to change External Vref during 2d Training
0xE089	Configure DCT For General use begin
0xE08A	Configure DCT For training begin
0xE08B	Configure DCT For Non-Explicit
0xE08C	Configure to Sync channels
0xE08D	Allocate C6 Storage
0xE08E	Before LV DDR4
0xE08F	Before LV DDR3
0xE090	TP0x90
0xE091	GNB earlier interface
0xE092	GNB Early VGA entry
0xE093	GNB Early VGA exit
0xE094	GNB Initialization entry
0xE095	GNB Initialization exit
0xE096	GNB internal debug code
0xE097	GNB internal debug code
0xE098	GNB internal debug code
0xE099	GNB internal debug code
0xE09A	GNB internal debug code
0xE09B	GNB internal debug code
0xE09C	GNB internal debug code
0xE09D	GNB internal debug code
0xE09E	GNB internal debug code
0xE09F	GNB internal debug code

0xE0A0	TP0xA0
0xE0A1	GNB internal debug code
0xE0A2	GNB internal debug code
0xE0A3	GNB internal debug code
0xE0A4	GNB internal debug code
0xE0A5	GNB internal debug code
0xE0A6	GNB internal debug code
0xE0A7	GNB internal debug code
0xE0A8	GNB internal debug code
0xE0A9	GNB internal debug code
0xE0AA	GNB internal debug code
0xE0AB	GNB internal debug code
0xE0AC	GNB internal debug code
0xE0AD	GNB internal debug code
0xE0AE	GNB internal debug code
0xE0AF	GNB internal debug code
New ABL Post Code Definitions	
These are temporary values until a new assignment is made	
0xEA00	ABL Begin
0xEA01	ABL End
0xEA10	ABL Debug Synchronization
0xE0B0	Abl1Begin
0xE0B1	ABL 1 Initialization
0xE0B2	ABL 1 DF Early
0xE0B3	ABL 1 DF Pre Training
0xE0B4	ABL 1 Debug Synchronization
0xE0B5	ABL 1 Error Detected
0xE0B6	ABL 1 Global memory error detected
0xE0B7	ABL 1 End
0xE0B8	ABL 2 Begin
0xE0B9	ABL 2 Initialization
0xE0BA	ABL 2 After Training
0xE0BB	ABL 2 Debug Synchronization
0xE0BC	ABL 2 Error detected
0xE0BD	ABL 2 Global memory error detected
0xE0BE	ABL 2 End
0xE0BF	ABL 3 Begin
0xE0C0	ABL 3 Initialziation
0xE1C0	ABL 3 GMI/xGMI Initialization Stage 1
0xB1C0	ABL 3 GMI/xGMI Initialization Stage 1 Warning
0xF1C0	ABL 3 GMI/xGMI Initialization Stage 2 Error
0xE2C0	ABL 3 GMI/xGMI Initialization Stage 2
0xB2C0	ABL 3 GMI/xGMI Initialization Stage 2 Warning
0xF2C0	ABL 3 GMI/xGMI Initialization Stage 2 Error
0xE3C0	ABL 3 GMI/xGMI Initialization Stage 3
0xB3C0	ABL 3 GMI/xGMI Initialization Stage 3 Warning
0xF3C0	ABL 3 GMI/xGMI Initialization Stage 3 Error
0xE4C0	ABL 3 GMI/xGMI Initialization Stage 4

0xB4C0	ABL 3 GMI/xGMI Initialization Stage 4 Warning
0xF4C0	ABL 3 GMI/xGMI Initialization Stage 4 Error
0xE5C0	ABL 3 GMI/xGMI Initialization Stage 5
0xB5C0	ABL 3 GMI/xGMI Initialization Stage 5 Warning
0xF5C0	ABL 3 GMI/xGMI Initialization Stage 5 Error
0xE6C0	ABL 3 GMI/xGMI Initialization Stage 6
0xB6C0	ABL 3 GMI/xGMI Initialization Stage 6 Warning
0xF6C0	ABL 3 GMI/xGMI Initialization Stage 6 Error
0xE7C0	ABL 3 GMI/xGMI Initialization Stage 7
0xE8C0	ABL 3 GMI/xGMI Initialization Stage 8
0xE9C0	ABL 3 GMI/xGMI Initialization Stage 9
0xF9C0	ABL 3 GMI/xGMI Initialization Stage 9 Error
0xEAC0	ABL 3 GMI/xGMI Initialization Stage 10
0xFAC0	ABL 3 GMI/xGMI Initialization Stage 10 Error
0xE0C1	Abl3ProgramUmcKeys
0xE0C2	ABL 3 DF Final Initalization
0xE0C3	ABL 3 Execute Synchronization Function
0xE0C4	ABL 3 Debug Synchronization Function
0xE0C5	ABL 3 Error Detected
0xE0C6	ABL 3 Global memroy error detected
0xE0C7	ABL 4 Initialiation - cold boot
0xE0C8	ABL 4 Memory test - cold boot
0xE0C9	ABL 4 APOB Initialization - cold boot
0xE0CA	ABL 4 Finalize memory settings - cold boot
0xE0CB	ABL 4 CPU Initialize Optimized Boot - cold boot
0xE0CC	ABL 4 Gmi Pcie Training - cold boot
0xE0CD	ABL 4 Cold boot End
0xE0CE	ABL 4 Initialization - Resume boot
0xE0CF	ABL 4 Resume End
0xE0D0	ABL 4 End Cold/Resume boot
0xE0D1	ABL 2 memory initialization
0xE0D2	ABL 3 memory initialization
0xE0D3	ABL 3 End
0xE0D4	ABL 1 Enter Memory Flow
0xE0D5	Memorry flow memory clock synchronization
0xE0E0	Before IDS calls out to get IDS data
0xE0E1	After IDS calls out to get IDS data
PMU test points	
0xE0F9	Failed PMU training.
0xE0FA	End of phase 1 memory code
0xE0FB	End of phase 2 memory code
ABL0 test points	
0xE0FC	Abl0Begin
0xE0FD	ABL 0 End
0xE0FE	Abl0 Begin with Fatal Mode
0xE0FF	ABL 0 End with Fatal Mode

ABL5 test points	
0xE100	ABL 7 End
0xE101	ABL 7 Resume boot
0xE102	ABL 6 End
0xE103	ABL 6 Initialization
0xE104	End of phase 1b memory code
0xE105	ABL 1b memory initialization
0xE106	ABL 6 Global memroy error detected
0xE107	ABL 1b Debug Synchronization Function
0xE108	ABL 4b Debug Synchronization Function
0xE109	AblbBegin
0xE10A	Ab4bBegin
0xE10B	BSP encountered HMAC fail on APOB Header
0xE10C	ABL 18 End
0xE10D	ABL 18 Resume boot
0xE10E	ABL 15 End
0xE10F	ABL 15 Initialization
0xE110	Before UMC based device initialization
0xE111	After UMC based device initialization
0xE2A0	ABL Error General ASSERT
0xE2A1	Unknown Error
0xE2A3	ABL Error Log Inig Error
0xE2A4	ABL Error for On DIMM thermal Heap allocation error
0xE2A5	ABL Error for memory test error
0xE2A6	ABL Error while executing memory test error
0xE2A7	ABL Error DDR Post Packge Repair Mem Auto Heap Alloc error
0xE2A8	ABL Error for DDR Post Package repair Apob Heap Alloc error
0xE2A9	ABL Error for DDR Post Package Repair No PPR Table Heap Aloc error
0xE2AA	ABL Error for Ecc Mem Auto Aloc Error error
0xE2AB	ABL Error for Soc Scan Heap Aloc error
0xE2AC	ABL Error for Soc Scan No Die error
0xE2AD	ABL Error for Nb Tech Heap Aloc error
0xE2AE	ABL Error for No Nb Constructor error
0xE2B0	ABL Error for No Tech Constructor error
0xE2B1	ABL Error for ABL1b Auto Alocation error
0xE2B2	ABL Error for ABL1b No NB Constructor error
0xE2B3	ABL Error for ABL2 No Nb Constructor error
0xE2B4	ABL Error for ABL3 Auto Allocation error
0xE2B5	ABL Error for ABL3 No Nb Constructor error
0xE2B6	ABL Error for ABL1b General error
0xE2B7	ABL Error for ABL2 General error
0xE2B8	ABL Error for ABL3 General error
0xE2B9	ABL Error for Get Target Speed error
0xE2BA	ABL Error for Flow P1 Family Support error
0xE2BB	ABL Error for No Valid Ddr4 Dimms error
0xE2BC	ABL Error for No Dimm Present error
0xE2BD	ABL Error for Flow P2 Family Supprot error
0xE2BE	ABL Error for Heap Deallocation for PMU Sram Msg Block error

0xE2BF	ABL Error for DDR Recovery error
0xEBC0	ABL Error for RRW Test error
0xE2C1	ABL Error for On Die Thermal error
0xE2C2	ABL Error for Heap Allocation For Dct Struct Amd Ch Def structure error
0xE2C3	ABL Error for Heap Allocation for PMU SRAM Msg block error
0xE2C4	ABL Error for Heap Phy PLL lock Flure error
0xE2C5	ABL Error for Pmu Training error
0xE2C6	ABL Error for Failure to Load or Verify PMU FW error
0xE2C7	ABL Error for Allocate for PMU SRAM Msg Block No Init error
0xE2C8	ABL Error for Failure BIOS PMU FW Mismatch AGESA PMU FW version error
0xE2C9	ABL Error for Agesa memory test error
0xE2CA	ABL Error for Deallocate for PMU SRAM Msg Block error
0xE2CB	ABL Error for Module Type Mismatch RDIMM error
0xE2CC	ABL Error for Module type Mismatch LRDIMM error
0xE2CD	ABL Error for MEm Auto NVDIM error
0xE2CE	ABL Error for Unknowm Responce error
0xE2CF	ABL Error for Over Clock Error RRW Test Results Error
0xE2D0	ABL Error for Over Clock Error PMU Training Error
0xE2D1	ABL Error for ABL1 General Error
0xE2D2	ABL Error for ABL2 General Error
0xE2D3	ABL Error for ABL3 General Error
0xE2D4	ABL Error for ABL4 General Error
0xE2D5	ABL Error over clock Mem Init Error
0xE2D6	ABL Error over clock Mem Other Error
0xE2D7	ABL Error for ABL6 General Error
0xE2D8	ABL Error Event Log Error
0xE2D9	ABL Error FATAL ABL1 Log Error
0xE2DA	ABL Error FATAL ABL2 Log Error
0xE2DB	ABL Error FATAL ABL3 Log Error
0xE2DC	ABL Error FATAL ABL4 Log Error
0xE2DD	ABL Error Slave Sync function execution Error
0xE2DE	ABL Error Slave Sync communicaton with data set to master Error
0xE2DF	ABL Error Slave broadcast communication from master to slave Error
0xE2E0	ABL Error FATAL ABL6 Log Error
0xE2E1	ABL Error Slave Offline Error
0xE2E2	ABL Error Slave Informs Master Error Info Error
0xE2E3	ABL Error Error Heap Locate for PMU SRAM Msg Block Error
0xE2E4	ABL Error ABL2 Auto Error
0xE2E5	ABL Error Flow P3 Family support Error
0xE2E5	ABL Error Abl 4 Gen Error
0xE2E7	ABL Error Mix RDIMM & LRDIMM in a channel
0xE2E8	ABL Error Memory Present on Disconnected Channel
0xE2EB	ABL Error MBIST Heap Allocation Error
0xE2EC	ABL Error MBIST Results Error
0xE2ED	ABL Error NO Dimm Smcus Info Error
0xE2EE	ABL Error Por Max Freq Table Error

0xE2EF	ABL Error Unsupproted DIMM Config Error
0xE2F0	ABL Error No Ps Table Error
0xE2F1	ABL Error Cad Bus Timing Not Found Error
0xE2F2	ABL Error Data Bus Timing Not Found Error
0xE2F3	ABL Error LrDIMM IBT Not Found Error
0xE2F4	ABL Error Unsupprote Dimm Config Max Freq Error Error
0xE2F5	ABL Error Mr0 Not Found Error
0xE2F6	ABL Error Obt Pattern Not found Error
0xE2F7	ABL Error Rc10 Op Speed Not FOund Error
0xE2F8	ABL Error Rc2 Ibt Not Found Error
0xE2F9	ABL Error Rtt Not Found Error
0xE2FA	ABL Error Checksum ReStrt Results Error
0xE2FB	ABL Error No Chipselect Results Error
0xE2FC	ABL Error No Common Cas Latency Results Error
0xE2FD	ABL Error Cas Latecncy exceeds Taa Max Error
0xE2FE	ABL Error Nvdimm Arm Missmatch Power Policy Error
0xE2FF	ABL Error Nvdimm Arm Missmatch Power Source Error
0xE300	ABL Error ABL 1 Mem Init Error
0xE301	ABL Error ABL 2 Mem Init Error
0xE302	ABL Error ABL 4 Mem Init Error
0xE303	ABL Error ABL 6 Mem Init Error
0xE304	ABL Error ABL 1 error repor Error
0xE305	ABL Error ABL 2 error repor Error
0xE306	ABL Error ABL 3 error repor Error
0xE307	ABL Error ABL 4 error repor Error
0xE308	ABL Error ABL 6 error repor Error
0xE30A	ABL Error message slave sync function execution Error
0xE30B	ABL Error slave offline Error
0xE30C	ABL Error Sync Master Error
0xE30D	ABL Error Slave Informs Master Info Message Error
0xE30E	ABL Error Mix Hynix LRDIMM with other vendor LRDIMM in a channel
0xE30F	ABL Error General Assert Error
0xE310	ABL ErrorNo Dimms On Any Channel in sysem
0xE311	ABL Error for Shared Heap Aloc error
0xE312	ABL Error for Main Heap Aloc error
0xE313	ABL Error for Shared Heap loc error
0xE314	ABL Error for Main Heap loc error
0xE316	ABL Error No memory available in system
0xE320	0xE320
0xE321	ABL Error Mixed 3DS and Non-3DS DIMM in a channel
0xE322	ABL Error Mixed x4 and x8 DIMM in a channel
0xE323	ABL Memory MBIST Rrw default test
0xE324	ABL Memory MBIST Interface test
0xE325	ABL Memory MBIST DataEye
0xE326	ABL Memory Post Package Repair
0xE327	ABL Error S0i3 DF restore buffer Error
0xE328	ABL Error CPU OPN Mismatch in case of Multi Socket population
0xE329	Recoverable APCB Checksum Error

0xE32A	Fatal APCB Checksum Error
0xE32B	ABL Error BIST Failure
0xE32C	ABL Error DDR Type Mismatch DDR5 Error
0xE32D	ABL Error Mix DIMM with different ECC bit size in a channel
0xE32E	ABL Error No ability to recover I2C bus without power cycling the platform
0xE32F	ABL Error I2C reset failure
0xE330	ABL Error DDR Module Type Mismatch
0xE331	ABL Error PMIC Error
0xE332	ABL Error Incompatible OPN
0xE333	ABL Error No ability to recover I3C bus without power cycling the platform
0xE334	ABL Error I3C reset failure
0xE335	ABL Error Absence of either or both AC-Power GPIO or WLAN GPIO Apcb Data
0xE336	ABL Memory Heal BIST Start
0xE337	ABL Memory Heal BIST End
0xE338	ABL Memory Heal BIST Write
0xE339	ABL Memory Heal BIST Read
0xE33A	ABL Memory Heal BIST Repair
0xE33B	Timeout at PMFW SwitchToMemoryTrainingState
0xE33C	DIMM with RCD Montage version B1 detected
0xE33D	ABL DDR PMU training complete
0xE33E	Timeout at PMFW SwitchToMemoryTrainingState
0xE33F	DIMM with TI PMIC revision 1.1 (XTPS) detected
0xE343	ABL DDR DIMM SPD verify CRC failure
0xE344	ABL DDR DIMM SPD Invalid Field Value
0xE345	ABL Timeout to detect CPU OPN Mismatch in case of Multi Socket population
0xE346	ABL Error 3DS DIMM in a SP6 system
0xE351	ABL DDR Runtime Post Package Repair End
0xE60B	ABL Functions execute Before
0xE60C	ABL Functions execute
0xEFFF	EndAgesas

AMD AGESA POST Code

(FW output 2 bytes post code,but user only can see low byte on IPMI command output)

Post Code	Description
Universal Post Code	
0xA001	Universal ACPI entry
0xA002	Universal ACPI exit
0xA003	Universal ACPI abort
0xA004	Universal SMBIOS entry
0xA005	Universal SMBIOS exit
0xA006	Universal SMBIOS abort

[0xA1XX] For CZ only memory Post codes	
0xA101	Memory structure initialization (Public interface)
0xA102	SPD Data processing (Public interface)
0xA103	Memory configuration (Public interface)
0xA104	DRAM initialization
0xA105	TpProcMemSPDChecking
0xA106	TpProcMemModeChecking
0xA107	Speed and TCL configuration
0xA108	TpProcMemSpdTiming
0xA109	TpProcMemDramMapping
0xA10A	TpProcMemPlatformSpecificConfig
0xA10B	TPProcMemPhyCompensation
0xA10C	TpProcMemStartDcts
0xA10D	(Public interface)
0xA10E	TpProcMemPhyFenceTraining
0xA10F	TpProcMemSynchronizeDcts
0xA110	TpProcMemSystemMemoryMapping
0xA111	TpProcMemMtrrConfiguration
0xA112	TpProcMemDramTraining
0xA113	(Public interface)
0xA114	TpProcMemWriteLevelizationTraining
0xA115	Below 800Mhz first pass start
0xA116	Above 800Mhz second pass start
0xA117	Target DIMM configured
0xA118	Prepare DIMMS for WL
0xA119	Configure DIMMS for WL
0xA11A	TpProcMemReceiverEnableTraining
0xA11B	Start sweep loop
0xA11C	Set receiver Delay
0xA11D	Write test pattern
0xA11E	Read test pattern
0xA11F	Compare test pattern
0xA120	Calculate MaxRdLatency per channel
0xA121	TpProcMemReceiveDqsTraining
0xA122	Set Write Data delay
0xA123	Write test pattern
0xA124	Start read sweep
0xA125	Set Receive DQS delay
0xA126	Read Test pattern
0xA127	Compare Test pattern
0xA128	Update results
0xA129	Start Find passing window
0xA12A	TpProcMemTransmitDqsTraining
0xA12B	Start write sweep
0xA12C	Set Transmit DQ delay
0xA12D	Write test pattern
0xA12E	Read Test pattern
0xA12F	Compare Test pattern

0xA130	Update results
0xA131	Start Find passing window
0xA132	TpProcMemMaxRdLatencyTraining
0xA133	Start sweep
0xA134	Set delay
0xA135	Write test pattern
0xA136	Read Test pattern
0xA137	Compare Test pattern
0xA138	Online Spare init
0xA139	Bank Interleave Init
0xA13A	Node Interleave Init
0xA13B	Channel Interleave Init
0xA13C	ECC initialization
0xA13D	Platform Specific Init
0xA13E	Before callout for "AgesaReadSpd"
0xA13F	After callout for "AgesaReadSpd"
0xA140	Before optional callout "AgesaHookBeforeDramInit"
0xA141	After optional callout "AgesaHookBeforeDramInit"
0xA142	Before optional callout "AgesaHookBeforeDQSTraining"
0xA143	After optional callout "AgesaHookBeforeDQSTraining"
0xA144	Before optional callout "AgesaHookBeforeDramInit"
0xA145	After optional callout "AgesaHookBeforeDramInit"
0xA146	After MemDataInit
0xA147	Before InitializeMCT
0xA148	Before LV DDR3
0xA149	Before InitMCT
0xA14A	Before OtherTiming
0xA14B	Before UMAMemTyping
0xA14C	Before SetDqsEccTmgs
0xA14D	Before MemClr
0xA14E	Before On DIMM Thermal
0xA14F	Before DMI
0xA150	End of memory code
0xA151	Entry point S3Init
0xA180	Sending MRS2
0xA181	Sedding MRS3
0xA182	Sending MRS1
0xA183	Sending MRS0
0xA184	Continuous Pattern Read
0xA185	Continuous Pattern Write
0xA186	Mem: 2d RdDqs Training begin
0xA187	Mem: Before optional callout to platform BIOS to change External Vref during 2d Training
0xA188	Mem: After optional callout to platform BIOS to change External Vref during 2d Training
0xA189	Configure DCT For General use begin
0xA18A	Configure DCT For training begin
0xA18B	Configure DCT For Non-Explicit

0xA18C	Configure to Sync channels
0xA18D	Allocate C6 Storage
0xA18E	Before LV DDR4
BR CPU	
0xA190	BR before AP launch
0xA191	Install AP launched PPI
0xA192	BR after AP launch
0xA193	Before CPU PM
0xA194	Enable IO Cstate
0xA195	Enable C6
0xA196	Install CCX PEI complete PPI
0xA197	BR CPU memory done call back entry
0xA198	Before APM weights
0xA199	0xA199
0xA19A	BR CPU memory done call back end
0xA19B	BR Init Mid entry
0xA19C	BR enable APM
0xA19D	BR Init Mid install protocol
0xA19E	BR Init Mid end
0xA19F	BR Init Late entry
0xA1A0	BR Init Late install protocol
0xA1A1	BR Init Late end
0xA1A2	BR DXE install complete protocol
0xA1A3	UNB install complete PPI
0xA1A4	UNB AfterApLaunch callback entry
0xA1A5	UNB AfterApLaunch callback end
S3 Interface Post Code	
0xA1EC	Before the S3 save code calls out to allocate a buffer
0xA1ED	After the S3 save code calls out to allocate a buffer
0xA1EE	Before the memory S3 save code calls out to allocate a buffer
0xA1EF	After the memory S3 save code calls out to allocate a buffer
0xA1F0	Before the memory code calls out to locate a buffer
0xA1F1	After the memory code calls out to locate a buffer
0xA1F2	Before the memory code calls out to locate a buffer
0xA1F3	After the memory code calls out to locate a buffer
0xA1F4	Before the memory code calls out to locate a buffer
0xA1F5	After the memory code calls out to locate a buffer
0xA1F6	Before the memory code calls out to locate a buffer
0xA1F7	After the memory code calls out to locate a buffer
PMU Post Code	
0xA1F9	Failed PMU training.
PSP V1 Modules	
0xA501	PspPeiV1 entry
0xA502	PspPeiV1 exit
0xA503	MemoryDiscoveredPpiCallback entry
0xA504	MemoryDiscoveredPpiCallback exit
0xA507	PspDxeV1 entry
0xA508	PspDxeV1 exit

0xA50A	PspDxeV1 PspPciEnumerationCompleteCallBack entry
0xA50B	PspDxeV1 PspPciEnumerationCompleteCallBack exit
0xA50C	PspDxeV1 ready to boot entry
0xA50D	PspDxeV1 ready to boot exit
0xA50E	PspSmmV1 entry
0xA50F	PspSmmV1 exit
0xA510	PspSmmV1 SwSmiCallBack entry, build the S3 save area for resume
0xA511	PspSmmV1 SwSmiCallBack exit, build the S3 save area for resume
0xA512	PspSmmV1 BspSmmResumeVector entry
0xA513	PspSmmV1 BspSmmResumeVector exit
0xA514	PspSmmV1 ApSmmResumeVector entry
0xA515	PspSmmV1 ApSmmResumeVector exit
0xA516	PspP2CmboxV1 entry
0xA517	PspP2CmboxV1 exit
PSP V2 Modules	
0xA521	PspPeiV2 entry
0xA522	PspPeiV2 exit
0xA523	PspDxeV2 entry
0xA524	PspDxeV2 exit
0xA525	PspDxeV2 PspMpServiceCallBack entry
0xA526	PspDxeV2 PspMpServiceCallBack exit
0xA527	PspDxeV2 FlashAccCallBack entry
0xA528	PspDxeV2 FlashAccCallBack exit
0xA529	PspDxeV2 ready to boot entry
0xA52A	PspDxeV2 ready to boot exit
0xA52B	PspDxeV2 exit boot serivce entry
0xA52C	PspDxeV2 exit boot serivce exit
0xA52D	PspSmmV2 entry
0xA52E	PspSmmV2 exit
0xA52F	PspSmmV2 SwSmiCallBack entry, build the S3 save area for resume
0xA530	PspSmmV2 SwSmiCallBack exit, build the S3 save area for resume
0xA531	PspSmmV2 BspSmmResumeVector entry
0xA532	PspSmmV2 BspSmmResumeVector exit
0xA533	PspSmmV2 ApSmmResumeVector entry
0xA534	PspSmmV2 ApSmmResumeVector exit
0xA535	PspP2CmboxV2 entry
0xA536	PspP2CmboxV2 exit
0xA537	TpPspRecoverApcbFail
0xA539	PspDxeV2 ApcbAccCallBack entry
0xA53A	PspDxeV2 ApcbAccCallBack exit
0xA53B	Enable Rd Instruction Fail
0xA53C	ScpcAutoEnablement failed due a variable with larger size detected
0xA53D	ScpcAutoEnablement failed due SetVariable
0xA53E	ScpcAutoEnablement failed due delete variable
0xA53F	C2P mailbox status field return with error, non-zero value

PSP fTpm modules	
0xA540	PspfTpmPei entry
0xA541	PspfTpmPei exit
0xA542	PspfTpmPei memory callback entry
0xA543	PspfTpmPei memory callback exit
0xA544	PspfTpmDxe entry
0xA545	PspfTpmDxe exit
PSP dTpm modules	
0xA546	PspdTpmPei entry
0xA547	PspdTpmPei exit
HSP fTpm modules	
0xA548	HspfTpmPei entry
0xA549	HspfTpmPei exit
0xA54A	HspfTpmPei Initialize Entry
0xA54B	HspfTpmPei Initialize Exit
0xA54C	HspfTpmDxe entry
0xA54D	HspfTpmDxe exit
Intrusion Detection [0xA56X]	
0xA560	PspIntrusionDetectionPei Entry
0xA561	PspIntrusionDetectionPei Exit
0xA562	PspIntrusionDetectionDxe Entry
0xA563	PspIntrusionDetectionDxe Exit
0xA564	Psp DoIntrusionDetectionAction in Dxe
0xA565	Psp IntrusionDetection Clear Tpm
0xA566	PspIntrusionDetectionSmm Entry
0xA567	PspIntrusionDetectionSmm Exit
0xA568	Psp IntrusionDetectionSmiCallback
0xA569	Psp DoIntrusionDetectionAction in Smm
0xA56E	Psp Intrusion Event Logging Error
0xA56F	Psp Intrusion Get Event Log Error
0xA570	Psp has got Async Cmd from the mailbox, but the routine is still running now
P2C mailbox Handling [0xA59X]	
0xA591	PspP2Cmbox Command SpiGetAttrib Handling entry
0xA592	PspP2Cmbox Command SpiSetAttrib Handling entry
0xA593	PspP2Cmbox Command SpiGetBlockSize Handling entry
0xA594	PspP2Cmbox Command SpiReadFV Handling entry
0xA595	PspP2Cmbox Command SpiWriteFV Handling entry
0xA596	PspP2Cmbox Command SpiEraseFV Handling entry
0xA598	PspP2Cmbox Command MboxPspCmdRpmcIncMc entry
0xA599	PspP2Cmbox Command TpMboxPspCmdRpmcReqMc entry
0xA59A	PspP2Cmbox Command TpMboxPspCmdArsStatus entry
0xA59B	PspP2Cmbox Command TpMboxPspCmdAsyncCmdDone entry
0xA59E	PspP2Cmbox Command Handling exit
0xA59F	PspP2Cmbox Command Handling Fail exit

fTPM command Handling [0xA5FX]	
0xA5F0	PspfTpm send TPM command entry
0xA5F1	PspfTpm send TPM command exit
0xA5F2	PspfTpm receive TPM command entry
0xA5F3	PspfTpm receive TPM command exit
0xA5F4	HspfTpm send TPM command entry
0xA5F5	HspfTpm send TPM command exit
0xA5F6	HspfTpm receive TPM command entry
0xA5F7	HspfTpm receive TPM command exit
C2P mailbox Handling [0xA601 ~ 0xA67F: before send C2P command, 0xA681 ~ 0xA6FF: wait C2P command]	
0xA600	PSP C2P mailbox entry base [0xA600 | Cmd]
0xA600	C2P command done, post code reused from TpPspC2PmboxBeforeSendCmdBase
0xA601	Before send C2P command MboxBiosCmdDramInfo
0xA602	Before send C2P command MboxBiosCmdSmmInfo
0xA603	Before send C2P command MboxBiosCmdSxInfo
0xA604	Before send C2P command MboxBiosCmdRsmInfo
0xA605	Before send C2P command MboxBiosCmdFtpmQuery
0xA606	Before send C2P command MboxBiosCmdBootDone
0xA607	Before send C2P command MboxBiosCmdClearS3Sts
0xA608	Before send C2P command MboxBiosS3DataInfo
0xA609	Before send C2P command MboxBiosCmdNop
0xA614	Before send C2P command MboxBiosCmdHSTIQuery
0xA619	Before send C2P command MboxBiosCmdGetVersion
0xA61B	Before send C2P command MboxBiosCmdLockDFReg
0xA61C	Before send C2P command MboxBiosCmdClrSmmLock
0xA61D	Before send C2P command MboxBiosCmdSetApCsBase
0xA61E	Before send C2P command MboxBiosCmdKvmInfo
0xA61F	Before send C2P command MboxBiosCmdLockSpi
0xA620	Before send C2P command MboxBiosCmdScreenOnGpio
0xA621	Before send C2P command MboxBiosCmdSpiOpWhiteList
0xA622	Before send C2P command MboxBiosCmdRasEinj
0xA624	Before send C2P command MboxBiosCmdStartArs
0xA625	Before send C2P command MboxBiosCmdStopArs
0xA626	Before send C2P command MboxBiosCmdSetBootPartitionId
0xA627	Before send C2P command MboxBiosCmdPspCapsQuery
0xA628	Before send C2P command MboxBiosCmdArmorEnterSmmOnlyMode
0xA629	Before send C2P command MboxBiosCmdArmorEnforceWhitelist
0xA62A	Before send C2P command MboxBiosCmdArmorExecuteSpiCommand
0xA62B	0xA62B
0xA62C	Before send C2P command MboxBiosCmdDrtmInfoId
0xA62D	Before send C2P command MboxBiosCmdLaterSplFuse
0xA62E	Before send C2P command MboxBiosCmdDtpmInfo
0xA62F	Before send C2P command MboxBiosCmdValidateManOsSignature
0xA630	Before send C2P command MboxBiosCmdLockFCHReg
0xA631	Before send C2P command MboxBiosCmdPostDrtmInfoQuery

0xA634	Before send C2P command MboxBiosCmdSignValidateHmacDataPreSmm
0xA635	Before send C2P command MboxBiosCmdSignValidateHmacDataSmm
0xA636	Before send C2P command MboxBiosCmdGetBootPartitionId
0xA639	Before send C2P command MboxBiosCmdSetRpmcAddress
0xA63A	Before send C2P command MboxBiosCmdSetGpioFencing
0xA63F	Before send C2P command MboxBiosCmdSendIvrsAcpiTable
0xA640	Before send C2P command MboxBiosCmdTa
0xA641	Before send C2P command MboxBiosCmdAcpiRasEinj
0xA642	Before send C2P command MboxBiosCmdQueryTCGLog
0xA647	Before send C2P command MboxBiosCmdQuerySplFuse
0xA649	Before send C2P command MboxBiosCmdManageabilityCfg
0xA64A	Before send C2P command MboxBiosCmdDisablePsb
0xA64B	Before send C2P command MboxBiosCmdUsbConfig
0xA64D	Before send C2P command MboxBiosCmdMpmPciAccess
0xA64F	Before send C2P command MboxBiosCmdStbVerbosity
0xA650	Before send C2P command MboxBiosCmdArmorEnterSmmOnlyMode2
0xA651	Before send C2P command MboxBiosCmdArmorSpiTransaction
0xA652	Before send C2P command MboxBiosCmdDeferredPsbFuse
0xA653	Before send C2P command MboxBiosCmdLoadWlanFw
0xA654	Before send C2P command MboxBiosCmdQuerySplValue
0xA680	PSP C2P mailbox exit base [0xA680 | Cmd]
0xA681	Wait C2P command MboxBiosCmdDramInfo finished
0xA682	Wait C2P command MboxBiosCmdSmmInfo finished
0xA683	Wait C2P command MboxBiosCmdSxInfo finished
0xA684	Wait C2P command MboxBiosCmdRsmInfo finished
0xA685	Wait C2P command MboxBiosCmdFtpmQuery finished
0xA686	Wait C2P command MboxBiosCmdBootDone finished
0xA687	Wait C2P command MboxBiosCmdClearS3Sts finished
0xA688	Wait C2P command MboxBiosS3DataInfo finished
0xA689	Wait C2P command MboxBiosCmdNop finished
0xA694	Wait C2P command MboxBiosCmdHSTIQuery finished
0xA699	Wait C2P command MboxBiosCmdGetVersion finished
0xA69B	Wait C2P command MboxBiosCmdLockDFReg finished
0xA69C	Wait C2P command MboxBiosCmdClrSmmLock finished
0xA69D	Wait C2P command MboxBiosCmdSetApCsBase finished
0xA69E	Wait C2P command MboxBiosCmdKvmInfo finished
0xA69F	Wait C2P command MboxBiosCmdLockSpi finished
0xA6A0	Wait C2P command MboxBiosCmdScreenOnGpio finished
0xA6A1	Wait C2P command MboxBiosCmdSpiOpWhiteList finished
0xA6A2	Wait C2P command MboxBiosCmdRasEinj finished
0xA6A4	Wait C2P command MboxBiosCmdStartArs finished
0xA6A5	Wait C2P command MboxBiosCmdStopArs finished
0xA6A6	Wait C2P command MboxBiosCmdSetBootPartitionId finished
0xA6A7	Wait C2P command MboxBiosCmdPspCapsQuery finished
0xA6A8	Wait C2P command MboxBiosCmdArmorEnterSmmOnlyMode finished

0xA6A9	Wait C2P command MboxBiosCmdArmorEnforceWhitelist finished
0xA6AA	Wait C2P command MboxBiosCmdArmorExecuteSpiCommand finished
0xA6AB	Wait C2P command MboxBiosCmdArmorSwitchCsMode finished
0xA6AC	Wait C2P command MboxBiosCmdDrtmInfoId finished
0xA6AD	Wait C2P command MboxBiosCmdLaterSplFuse finished
0xA6AE	Wait C2P command MboxBiosCmdDtpmInfo finished
0xA6AF	Wait C2P command MboxBiosCmdValidateManOsSignature finished
0xA6B0	Wait C2P command MboxBiosCmdLockFCHReg finished
0xA6B1	Wait C2P command MboxBiosCmdPostDrtmInfoQuery finished
0xA6B4	Wait C2P command MboxBiosCmdSignValidateHmacDataPreSmm finished
0xA6B5	Wait C2P command MboxBiosCmdSignValidateHmacDataSmm finished
0xA6B6	Wait C2P command MboxBiosCmdGetBootPartitionId finished
0xA6B9	Wait C2P command MboxBiosCmdSetRpmcAddress finished
0xA6BA	Wait C2P command MboxBiosCmdSetGpioFencing finished
0xA6BF	Wait C2P command MboxBiosCmdSendIvrsAcpiTable finished
0xA6C0	Wait C2P command MboxBiosCmdTa finished
0xA6C1	Wait C2P command MboxBiosCmdAcpiRasEinj finished
0xA6C2	Wait C2P command MboxBiosCmdQueryTCGLog finished
0xA6C7	Wait C2P command MboxBiosCmdQuerySplFuse finished
0xA6C9	Wait C2P command MboxBiosCmdManageabilityCfg finished
0xA6CA	Wait C2P command MboxBiosCmdDisablePsb finished
0xA6CB	Wait C2P command MboxBiosCmdUsbConfig finished
0xA6CD	Wait C2P command MboxBiosCmdMpmPciAccess finished
0xA6CF	Wait C2P command MboxBiosCmdStbVerbosity finished
0xA6D0	Wait C2P command MboxBiosCmdArmorEnterSmmOnlyMode2 finished
0xA6D1	Wait C2P command MboxBiosCmdArmorSpiTransaction finished
0xA6D2	Wait C2P command MboxBiosCmdDeferredPsbFuse finishe
0xA6D3	Wait C2P command MboxBiosCmdLoadWlanFw finished
0xA6D4	Wait C2P command MboxBiosCmdQuerySplValue finished
MPM related [0xA700 - 0xA77F]	
0xA700	MpmPei Driver entry
0xA701	MpmPei Driver exit
0xA702	MpmDxe Driver entry
0xA703	MpmDxe Driver exit
0xA704	MPM RTB event entry
0xA705	MPM RTB event exit
0xA706	Mpm Seriallo Entry
0xA707	Mpm Seriallo Exit
0xA708	TpMpmMoselleDxe Driver Entry
0xA709	TpMpmMoselleDxe Driver Exit
USB4 related [0xA780 - 0xA79F]	
0xA780	Usb4Pei Driver entry
0xA781	Usb4Pei Driver exit
0xA782	Usb4Pei MemoryDicoverPpiCallback entry

0xA783	Usb4Pei MemoryDicoverPpiCallback exit
0xA784	Usb4Dxe Driver entry
0xA785	Usb4Dxe Driver exit
[0xA900, 0xA94F] NBIO PEIM/DXE Driver	
0xA900	AmdNbioBase PEIM driver entry
0xA901	AmdNbioBase PEIM driver exit
0xA902	AmdNbioBase DXE driver entry
0xA903	AmdNbioBase DXE driver exit
PCIe	
0xA904	AmdNbioPcie PEIM driver entry
0xA905	AmdNbioPcie PEIM driver exit
0xA906	AmdNbioPcie DXE driver entry
0xA907	AmdNbioPcie DXE driver exit
GFX	
0xA908	AmdNbioGfx PEIM driver entry
0xA909	AmdNbioGfx PEIM driver exit
0xA90A	AmdNbioGfx DXE driver entr
0xA90B	AmdNbioGfx DXE driver exit
IOMMU	
0xA90C	AmdNbioIommu DXE driver entry
0xA90D	AmdNbioIommu DXE driver exit
ALIB	
0xA90E	AmdNbioALIB DXE driver entry
0xA90F	AmdNbioALIB DXE driver exit
SMU	
0xA910	AmdSmu PEI driver entry
0xA911	AmdSmu PEI driver exit
0xA912	AmdSmu DXE driver entry
0xA913	AmdSmu DXE driver exit
0xA914	SmuServiceRequest entry
0xA915	SmuServiceRequest exit
IOAPIC	
0xA916	AmdNbioIoApic PEI driver entry
0xA917	AmdNbioIoApic PEI driver exit
IOMMU PEIM	
0xA920	AmdNbioIommu PEIM driver entry
0xA921	AmdNbioIommu PEIM driver exit
APCB DXE	
0xA922	APCB DXE Entry
0xA923	APCB DXE Exit
APCB SMM	
0xA924	APCB SMM Entry
0xA925	APCB SMM Exit
0xA930	Early Exit
0xA931	Early Exit
0xA932	Early Training is completed

[0xA950, 0xA99F] NBIO PPI/PROTOCOL Callback	
0xA950	NbioTopologyConfigureCallback entry
0xA951	NbioTopologyConfigureCallback exit
0xA952	MemoryConfigDoneCallbackPpi entry
0xA953	MemoryConfigDoneCallbackPpi exit
0xA954	DxioInitializationCallbackPpi entry
0xA955	DxioInitializationCallbackPpi exit
0xA956	DispatchSmuV9Callback entry
0xA957	DispatchSmuV9Callback exit
0xA958	DispatchSmuV10Callback entry
0xA959	DispatchSmuV10Callback exit
0xA95A	AmdPcieMiscInit Event entry
0xA95B	AmdPcieMiscInit Event exit
0xA95C	NbioBaseHookReadyToBoot Event entry
0xA95D	NbioBaseHookReadyToBoot Event exit
0xA95E	NbioBaseHookPciIO Event entry
0xA95F	NbioBaseHookPciIO Event exit
0xA960	DispatchSmuV13Callback entry
0xA961	DispatchSmuV13Callback exit
[0xA980, 0xA99F] BR GNB task	
0xA970	GnbEarlyInterfaceCZ entry
0xA971	GnbEarlyInterfaceCZ exit
0xA972	PcieConfigurationInit entry
0xA973	PcieConfigurationInit exit
0xA974	GnbEarlierInterfaceCZ entry
0xA975	GnbEarlierInterfaceCZ exit
0xA976	PcieEarlyInterfaceCZ entry
0xA977	PcieEarlyInterfaceCZ exit
0xA978	PciePostEarlyInterfaceCZ entry
0xA979	PciePostEarlyInterfaceCZ exit
0xA97A	GfxConfigPostInterfaceCZ entry
0xA97B	GfxConfigPostInterfaceCZ exit
0xA97C	GfxPostInterfaceCZ entry
0xA97D	GfxPostInterfaceCZ exit
0xA97E	GnbPostInterfaceCZ entry
0xA97F	GnbPostInterfaceCZ exit
0xA980	PciePostInterfaceCZ entr
0xA981	PciePostInterfaceCZ exit
0xA982	GnbEnvInterfaceCZ entry
0xA983	GnbEnvInterfaceCZ exit
0xA984	GfxConfigEnvInterface entry
0xA985	GfxConfigEnvInterface exit
0xA986	GfxEnvInterfaceCZ entry
0xA987	GfxEnvInterfaceCZ exit
0xA988	GfxMidInterfaceCZ entry
0xA989	GfxMidInterfaceCZ exit
0xA98A	GfxIntInfoTableInterfaceCZ entry

0xA98B	GfxIntInfoTableInterfaceCZ exit
0xA98C	PcieMidInterfaceCZ entry
0xA98D	PcieMidInterfaceCZ exit
0xA98E	GnbMidInterfaceCZ entry
0xA98F	GnbMidInterfaceCZ exit
0xA990	GnbSmuMidInterfaceCZ entry
0xA991	GnbSmuMidInterfaceCZ exit
0xA992	InvokeAmdInitLate entry
0xA993	InvokeAmdInitLate exit
[0xAA80, 0xAAAF] Alib task	
0xAA80	ALib 0 entry
0xAA81	ALib 0 exit
0xAA82	ALib 1 entry
0xAA83	ALib 1 exit
0xAA84	ALib 2 entry
0xAA85	ALib 2 exit
0xAA86	ALib 3 entry
0xAA87	ALib 3 exit
0xAA88	ALib 6 entry
0xAA89	ALib 6 exit
0xAA8A	ALib A entry
0xAA8B	ALib A exit
0xAA8C	ALib B entry
0xAA8D	ALib B exit
0xAA8E	ALib C entry
0xAA8F	ALib C exit
0xAA90	ALib 10 entry
0xAA91	ALib 10 exit
0xAA92	ALib 11 entry
0xAA93	ALib 11 exit
0xAA94	ALib 12 entry
0xAA95	ALib 12 exit
0xAA96	ALib 13 entry
0xAA97	ALib 13 exit
0xAA98	ALib AA entry
0xAA99	ALib AA exit
[0xACXX] assigned for AGESA CCX Module	
0xAC10	CCX IDS IDS_HOOK_CCX_AFTER_AP_LAUNCH
0xAC50	CCX PEI entry
0xAC51	CCX downcore entry
0xAC55	CCX DXE entry
0xAC56	CCX MP service callback entry
0xAC57	CCX Ready To Boot callback entry
0xAC58	CCX oc service callback entry
0xAC5D	CCX SMM entry
0xAC70	CCX PEI start to launch APs for S3
0xAC71	CCX PEI end of launching APs for S3
0xAC90	CCX start to launch AP

0xAC91	CCX launch AP is ended
0xAC92	CCX launch AP abort
0xAC93	CCX MP service abort
0xAC94	CCX cac weights
0xAC95	CCX before install CcxDone
0xAC96	CCX after install CcxDone
0xAC97	CCX loaded microcode
0xACE0	CCX PEI exit
0xACE1	CCX downcore exit
0xACE5	CCX DXE exit
0xACE6	CCX MP service callback exit
0xACE7	CCX Ready To Boot callback exit
0xACE8	CCX OC service callback exit
0xACED	CCX SMM exit
[0xADXX] assigned for AGESA DF Module	
0xAD50	DF PEI entry
0xAD55	DF DXE entry
0xAD56	DF Ready to Boot entry
0xAD57	DF NbioSmuServicesPpiCallback entry
0xAD58	DF NbioSmuServicesProtocolCallback entry
0xAD59	DF SMM entry
0xAD60	DF FabricPciEnumerationCompleteCallBack entry
0xADE0	DF PEI exit
0xADE5	DF DXE exit
0xADE6	DF Ready to Boot exit
0xADE7	DF NbioSmuServicesPpiCallback exit
0xADE8	DF NbioSmuServicesProtocolCallback exit
0xADE9	DF SMM exit
0xADEA	DF FabricPciEnumerationCompleteCallBack exit
FCH	
0xAF01	FCH InitReset dispatch point
0xAF06	FCH InitEnv dispatch point
0xAF07	FCH InitMid dispatch point
0xAF08	FCH InitLate dispatch point
0xAF0B	FCH InitS3Early dispatch point
0xAF0C	FCH InitS3Late dispatch point
0xAF0D	FCH InitS3Early dispatch finished
0xAF0E	FCH InitS3Late dispatch finished
0xAF10	FCH Pei Entry
0xAF11	FCH Pei Exit
0xAF12	FCH MultiFch Pei Entry
0xAF13	FCH MultiFch Pei Exit
0xAF14	0xAF14
0xAF15	FCH Dxe Exit
0xAF16	FCH MultiFch Dxe Entry
0xAF17	FCH MultiFch Dxe Exit
0xAF18	FCH Smm Entry
0xAF19	FCH Smm Exit

0xAF20	FCH Smm Dispatcher Entry
0xAF21	FCH Smm Dispatcher Exit
0xAF40	FCH InitReset HwAcpi
0xAF41	FCH InitReset AB Link
0xAF42	FCH InitReset LPC
0xAF43	FCH InitReset SPI
0xAF44	FCH InitReset eSPI
0xAF45	FCH InitReset SD
0xAF46	FCH InitReset eMMC
0xAF47	FCH InitReset SATA
0xAF48	FCH InitReset USB
0xAF49	FCH InitReset xGbE
0xAF4A	FCH InitReset USB Ready
0xAF4B	FCH InitReset USB4 Ready
0xAF4E	FCH InitReset USB4
0xAF4F	FCH InitReset HwAcpiP
0xAF50	FCH InitEnv HwAcpi
0xAF51	FCH InitEnv AB Link
0xAF52	FCH InitEnv LPC
0xAF53	FCH InitEnv SPI
0xAF54	FCH InitEnv eSPI
0xAF55	FCH InitEnv SD
0xAF56	FCH InitEnv eMMC
0xAF57	FCH InitEnv SATA
0xAF58	FCH InitEnv USB
0xAF59	FCH InitEnv xGbE
0xAF5E	FCH InitEnv USB4
0xAF5F	FCH InitEnv HwAcpiP
0xAF60	FCH InitMid HwAcpi
0xAF61	FCH InitMid AB Link
0xAF62	FCH InitMid LPC
0xAF63	FCH InitMid SPI
0xAF64	FCH InitMid eSPI
0xAF65	FCH InitMid SD
0xAF66	FCH InitMid eMMC
0xAF67	FCH InitMid SATA
0xAF68	FCH InitMid USB
0xAF69	FCH InitMid xGbE
0xAF6E	FCH InitMid USB4
0xAF70	FCH InitLate HwAcpi
0xAF71	FCH InitLate AB Link
0xAF72	FCH InitLate LPC
0xAF73	FCH InitLate SPI
0xAF74	FCH InitLate eSPI
0xAF75	FCH InitLate SD
0xAF76	FCH InitLate eMMC
0xAF77	FCH InitLate SATA
0xAF78	FCH InitLate USB

0xAF79	FCH InitLate xGbE
0xAF7A	FCH PT load FW Entry
0xAF7B	FCH PT load FW Exit
0xAF7C	FCH PT_Plus load FW Entry
0xAF7D	FCH PT_Plus load FW Exit
0xAF7E	0xAF7E
0xAF7F	FCH PT Start to load FW
0xAF80	FCH Device Enter D x Status
0xAF81	FCH PT load FW Delay 1 sec
0xAF82	FCH PT load FW Delay 2 sec
0xAF83	FCH PT load FW Delay 3 sec
0xAF84	FCH PT load FW Delay 4 sec
0xAF85	FCH PT load FW Delay 5 sec
0xAF86	FCH PT load FW Delay 6 sec
0xAF87	FCH PT load FW Delay 7 sec
0xAF88	FCH PT load FW Delay 8 sec
0xAF89	FCH PT load FW Delay 9 sec
0xAF8A	FCH PT load FW Delay 10 sec
0xAF8B	FCH Secondary PT Start to load FW
0xAF90	FCH Turner Load FW Entry
0xAF91	FCH Turner Load FW Exit
0xAF92	FCH Turner Start to Load FW
0xAFB0	Bixby Pei Entry
0xAFB1	Bixby Pei Exit
0xAFB2	Bixby Dxe Entry
0xAFB3	Bixby Dxe Exit
0xAFB4	Bixby Smm Entry
0xAFB5	Bixby Smm Exit
0xAFB6	Bixby InitReset dispatch point
0xAFB7	Bixby InitMid dispatch point
0xAFB8	Bixby InitEnv dispatch point
0xAFB9	Bixby InitLate dispatch point
0xAFBA	Bixby InitS3Early dispatch point
0xAFBB	Bixby InitS3Late dispatch point
0xAFBC	Bixby InitS3Early dispatch finished
0xAFBD	Bixby InitS3Late dispatch finished
0xAFBE	Bixby InitReset SATA Entry
0xAFBF	Bixby InitReset SATA Exit
0xAFC0	Bixby InitMid SATA Entry
0xAFC1	Bixby InitMid SATA Exit
0xAFC2	Bixby InitEnv SATA Entry
0xAFC3	Bixby InitEnv SATA Exit
0xAFC4	Bixby InitLate SATA Entry
0xAFC5	Bixby InitLate SATA Exit
0xAFC6	Bixby InitReset USB Entry
0xAFC7	Bixby InitReset USB Exit
0xAFC8	Bixby InitMid USB Entry
0xAFC9	Bixby InitMid USB Exit

0xAFCA	Bixby InitEnv USB Entry
0xAFCB	Bixby InitEnv USB Exit
0xAFCC	Bixby InitLate USB Entry
0xAFCD	Bixby InitLate USB Exit
0xAFCE	Bixby InitEnv HwAcpiP
0xAFCF	Bixby InitReset HwAcpiP
0xAFFF	End of TP range for FCH
0xFFFF	Last defined AGESA PCs

AMI POST Code

Post Code	Description
0x10	PEI core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization is started (CPU module specific)
0x13	Pre-memory CPU initialization is started (CPU module specific)
0x14	Pre-memory CPU initialization is started (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-memory North Bridge initialization is started (North Bridge module specific)
0x17	Pre-memory North Bridge initialization is started (North Bridge module specific)
0x18	Pre-memory North Bridge initialization is started (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization is started (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization is started (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization is started (South Bridge module specific)
0x1D~ 0x2A	Oem pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect(SPD) data reading
0x2C	Memory initialization. Meory Presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization. (Other)
0x30	Reserved for ASL (See ASL status codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. BootStrap Processor(BSP) initialization
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-memory North Bridge initialization is started

0x38	Post-memory North Bridge initialization is started (North Bridge module specific)
0x39	Post-memory North Bridge initialization is started (North Bridge module specific)
0x3A	Post-memory North Bridge initialization is started (North Bridge module specific)
0x3B	Post-memory South Bridge initialization is started
0x3C	Post-memory South Bridge initialization is started (South Bridge module specific)
0x3D	Post-memory South Bridge initialization is started (South Bridge module specific)
0x3E	Post-memory South Bridge initialization is started (South Bridge module specific)
0x3F~0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
S3 resume progress codes	
0xE0	S3 Resume is started (S3 Resume PPI is called by th DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4~0xE7	Reserved for future AMI progress codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loadded
0xF5~0xF7	Reserved for future AMI progress codes
DXE Phase	
0x60	DXE code is started
0x61	NVRAM initialization
0x62	Initialization of the South Bridge runtimes services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Brodge module specific)
0x6C	North Bridge DXE initialization (North Brodge module specific)
0x6D	North Bridge DXE initialization (North Brodge module specific)
0x6E	North Bridge DXE initialization (North Brodge module specific)
0x6F	North Bridge DXE initialization (North Brodge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization

0x73	North Bridge DXE initialization (South Brodge module specific)
0x74	North Bridge DXE initialization (South Brodge module specific)
0x75	North Bridge DXE initialization (South Brodge module specific)
0x76	North Bridge DXE initialization (South Brodge module specific)
0x77	North Bridge DXE initialization (South Brodge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A~0x7F	Reserved for future AMI DXE codes
0x80~0x8F	OEM DXE initialization codes
0x90	Boot Device Selection(BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E~0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Satrt of Setup
0xAA	Reserved for ASL(See ASL Status Codes selection below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL(See ASL Status Codes selection below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM initialization
0xB3	System Reset
0xB4	USB Hot Plug
0xB5	PCI bus Hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reste (reset of NVRAM settings)

0xB8~0xBF	Reserved for future AMI codes
0xC0~0xCF	OEM BDS initialization codes
ACPI ASL Checkpoints	
0x01	System is entering S1 sleeping state
0x02	System is entering S2 sleeping state
0x03	System is entering S3 sleeping state
0x04	System is entering S4 sleeping state
0x05	System is entering S5 sleeping state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

Boot loader Error codes

Post Code	Description
0x00	General - Success
0x01	Generic Error Code
0x02	Generic Memory Error
0x03	Buffer Overflow
0x04	Invalid Parameter(s)
0x05	Invalid Data Length
0x06	Data Alignment Error
0x07	Null Pointer Error
0x08	Unsupported Function
0x09	Invalid Service ID
0x0A	Invalid Address
0x0B	Out of Resource Error
0x0C	Timeout
0x0D	data abort exception
0x0E	prefetch abort exception
0x0F	Out of Boundary Condition Reached
0x10	Data corruption
0x11	Invalid command
0x12	The package type provided by BR is incorrect
0x13	Failed to retrieve FW header during FW validation
0x14	Key size not supported
0x15	Agesa0 verification error
0x16	SMU FW verification error
0x17	OEM SINGING KEY verification error
0x18	Generic FW Validation error
0x19	RSA operation fail - bootloader
0x1A	CCP Passthrough operation failed - internal status
0x1B	AES operation fail

0x1C	CCP state save failed
0x1D	CCP state restore failed
0x1E	SHA256/384 operation fail - internal status
0x1F	ZLib Decompression operation fail
0x20	HMAC-SHA256/384 operation fail - internal status
0x21	Booted from boot source not recognized by PSP
0x22	PSP directory entry not found
0x23	PSP failed to set the write enable latch
0x24	PSP timed out because spirom took too long
0x25	Cannot find BIOS directory
0x26	SpiRom is not valid
0x27	slave die has different security state from master
0x28	SMI interface init failure
0x29	SMI interface generic error
0x2A	invalid die ID executes MCM related function
0x2B	invalid MCM configuration table read from bootrom
0x2C	Valid boot mode wasn't detected
0x2D	NVStorage init failure
0x2E	NVStorage generic error
0x2F	MCM 'error' to indicate slave has more data to send
0x30	MCM error if data size exceeds 32B
0x31	Invalid client id for SVC MCM call
0x32	MCM slave status register contains bad bits
0x33	MCM call was made in a single die environment
0x34	PSP secure mapped to invalid segment (should be 0x400_0000)
0x35	No physical x86 cores were found on die
0x36	Insufficient space for secure OS (range of free SRAM to SVC stack base)
0x37	SYSHUB mapping memory target type is not supported
0x38	Attempt to unmap permanently mapped TLB to PSP secure region
0x39	Unable to map an SMN address to AXI space
0x3A	Unable to map a SYSHUB address to AXI space
0x3B	The count of CCXs or cores provided by bootrom is not consistent
0x3C	Uncompressed image size doesn't match value in compressed header
0x3D	Compressed option used in case where not supported
0x3E	Fuse info on all dies don't match
0x3F	PSP sent message to SMU; SMU reported an error
0x40	Function RunPostX86ReleaseUnitTests failed in memcmp()
0x41	Interface between PSP to SMU not available.
0x42	Timer wait parameter too large
0x43	Test harness module reported an error
0x44	x86 wrote C2PMSG_0 interrupting PSP, but the command has an invalid format
0x45	Failed to read from SPI the Bios Directory or Bios Combo Directory
0x46	Failed to find FW entry in SPL Table
0x47	Failed to read the combo bios header
0x48	SPL version missmatch
0x49	Error in Validate and Loading AGESA APOB SVC call

0x4A	Correct fuse bits for DIAG_BL loading not set
0x4B	The UmcProgramKeys() function was not called by AGESA
0x4C	Unconditional Unlock based on serial numbers failure
0x4D	Syshub register programming mismatch during readback
0x4E	Family ID in MP0_SFUSE_SEC[7:3] not correct
0x4F	An operation was invoked that can only be performed by the GM
0x50	Failed to acquire host controller semaphore to claim ownership of SMB
0x51	Timed out waiting for host to complete pending transactions
0x52	Timed out waiting for slave to complete pending transactions
0x53	Unable to kill current transaction on host, to force idle
0x54	One of: Illegal command, Unclaimed cycle, or Host time out
0x55	An smbus transaction collision detected, operation restarted
0x56	Transaction failed to be started or processed by host, or not completed
0x57	An unsolicited smbus interrupt was received
0x58	An attempt to send an unsupported PSP-SMU message was made
0x59	An error/data corruption detected on response from SMU for sent msg
0x5A	MCM Steady-state unit test failed
0x5B	S3 Enter failed
0x5C	AGESA BL did not set PSP SMU reserved addresses via SVC call
0x5D	Reserved PSP/SMU memory region is invalid
0x5E	CcxSecBisiEn not set in fuse RAM
0x5F	Received an unexpected result
0x60	VMG Storage Init failed
0x61	failure in mbedTLS user app
0x62	An error occured whilst attempting to SMN map a fuse register
0x63	Fuse burn sequence/operation failed due to internal SOC error
0x64	Fuse sense operation timed out
0x65	Fuse burn sequence/operation timed out waiting for burn done
0x66	The PMU FW Public key certificate loading or authentication fails
0x67	This PSP FW was revoked
0x68	The platform model/vendor id fuse is not matching the BIOS public key token
0x69	The BIOS OEM public key of the BIOS was revoked for this platform
0x6A	PSP level 2 directory not match expected value.
0x6B	BIOS level 2 directory not match expected value.
0x6C	Reset image not found
0x6D	Generic error indicating the CCP HAL initialization failed
0x6E	failure to copy NVRAM to DRAM.
0x6F	Invalid key usage flag
0x70	Unexpected fuse set
0x71	RSMU signaled a security violation
0x72	Error programming the WAFL PCS registers
0x73	Error setting wafl PCS threshold value
0x74	Error loading OEM trustlets
0x75	Recovery mode accross all dies is not sync'd

0x76	Uncorrectable WAFL error detected
0x77	Fatal MP1 error detected
0x78	Bootloader failed to find OEM signature
0x79	Error copying BIOS to DRAM
0x7A	Error validating BIOS image signature
0x7B	OEM Key validation failed
0x7C	Platform Vendor ID and/or Model ID binding violation
0x7D	Bootloader detects BIOS request boot from SPI-ROM, which is unsupported for PSB.
0x7E	Requested fuse is already blown, reblow will cause ASIC malfunction
0x7F	Error with actual fusing operation
0x80	(Local Master PSP on P1 socket) Error reading fuse info
0x81	(Local Master PSP on P1 socket) Platform Vendor ID and/or Model ID binding violation
0x82	(Local Master PSP on P1 socket) Requested fuse is already blown, reblow will cause ASIC malfunction
0x83	(Local Master PSP on P1 socket) Error with actual fusing operation
0x84	SEV FW Rollback attempt is detected
0x85	SEV download FW command fail to broadcase and clear the IsInSRAM field on slave dies
0x86	Agesa error injection failure
0x87	Uncorrectable TWIX error detected
0x88	Error programming the TWIX PCS registers
0x89	Error setting TWIX PCS threshold value
0x8A	SW CCP queue is full, cannot add more entries
0x8B	CCP command description syntax error detected from input
0x8C	Return value stating that the command has not yet be scheduled
0x8D	The command is scheduled and being worked on
0x8E	The DXIO PHY SRAM Public key certificate loading or authentication fails
0x8F	fTPM binary size exceeds limit allocated in Private DRAM, need to increase the limit
0x90	The TWIX link for a particular CCD is not trained Fatal error
0x91	Security check failed (not all dies are in same security state)
0x92	FW type mismatch between the requested FW type and the FW type embedded in the FW binary header
0x93	SVC call input parameter address violation
0x94	Firmware Compatibility Level mismatch
0x95	Bad status returned by I2CKnollCheck
0x96	NACK to general call (no device on Knoll I2C bus)
0x97	Null pointer passed to I2CKnollCheck
0x98	Invalid device-ID found during Knoll authentication
0x99	Error during Knoll/Prom key derivation
0x9A	Null pointer passed to Crypto function
0x9B	Error in checksum from wrapped Knoll/Prom keys
0x9C	Knoll returned an invalid response to a command
0x9D	Bootloader failed in Knoll Send Command function
0x9E	No Knoll device found by verifying MAC
0x9F	The maximum allowable error post code

BL_TRACECODE	
0xA0	Bootloader successfully entered C Main
0xA1	Master initialized C2P / slave waited for master to init C2P
0xA2	HMAC key successfully derived
0xA3	Master got Boot Mode and sent boot mode to all slaves
0xA4	SpiRom successfully initialized
0xA5	BIOS Directory successfully read from SPI to SRAM
0xA6	Early unlock check
0xA7	Inline Aes key successfully derived
0xA8	Inline-AES key programming is done
0xA9	Inline-AES key wrapper derivation is done
0xAA	Bootloader successfully loaded HW IP configuration values
0xAB	Bootloader successfully programmed MBAT table
0xAC	Bootloader successfully loaded SMU FW
0xAE	User mode test Uapp completed successfully
0xAF	Bootloader loaded Agesa0 from SpiRom
0xB0	AGESA phase has completed
0xB1	RunPostDramTrainingTests() completed successfully
0xB2	SMU FW Successfully loaded to SMU Secure DRAM
0xB3	Sent all required boot time messages to SMU
0xB4	Validated and ran Security Gasket binary
0xB5	UMC Keys generated and programmed
0xB6	Inline AES key wrapper stored in DRAM
0xB7	Completed FW Validation step
0xB8	Completed FW Validation step
0xB9	BIOS copy from SPI to DRAM complete
0xBA	Completed FW Validation step
0xBB	BIOS load process fully complete
0xBC	Bootloader successfully release x86
0xBD	Early Secure Debug completed
0xBE	GetFWVersion command received from BIOS is completed
0xBF	SMIInfo command received from BIOS is completed
0xC0	Successfully entered WarmBootResume()
0xC1	Successfully copied SecureOS image to SRAM
0xC2	Successfully copied trustlets to PSP Secure Memory
0xC3	About to jump to Secure OS (SBL about to copy and jump)
0xC4	Successfully restored CCP and UMC state on S3 resume
0xC5	PSP SRAM HMAC validated by Mini BL
0xC6	About to jump to <t-base in Mini BL
0xC7	VMG ECDH unit test started
0xC8	VMG ECDH unit test passed
0xC9	VMG ECC CDH primitive unit test started
0xCA	VMG ECC CDH primitive unit test passed
0xCB	VMG SP800-108 KDF-CTR HMAC unit test starte
0xCC	VMG SP800-108 KDF-CTR HMAC unit test passed
0xCD	VMG LAUNCH_* test started
0xCE	VMG LAUNCH_* test passed
0xCF	MP1 has been taken out of reset, and executing SMUFW

0xD0	PSP and SMU Reserved Addresses correct
0xD1	Reached Naples steady-state WFI loop
0xD2	Knoll device successfully initialized
0xD3	32-byte RandOut successfully returned from Knoll
0xD4	32-byte MAC successfully received from Knoll.
0xD5	Knoll device verified successfully
0xD6	CNLI Keys generated and programmed
0xD7	Enter recovery mode due to trustlet validation fail.
0xD8	Enter recovery mode due to OS validation fail.
0xD9	Enter recovery mode due to OEM public key not found.
0xDA	Enter recovery mode with header corruption
0xDB	We should not treat this error as blocking
0xDC	When same fw image type is already loaded in SRAM
0xE0	Unlock return
0xE2	Token exipration reset triggered
0xE3	Completed DXIO PHY SRAM FW key Validation step
0xE4	MP1 firmware load to SRAM success
0xE5	Bootloader read the MP1 SRAM successfully
0xE6	Bootloader successfully reset MP1
0xE7	DF init successfully done (in absence of AGESA)
0xE8	UMC init successfully done (in absence of AGESA)
0xE9	LX6 Boot ROM code ready
0xEA	Bootloader successfully asserted LX6 reset
0xEB	LX6 load to SRAM success
0xEC	Bootloader successfully set LX6 reset vector to SRAM
0xED	Bootloader successfully de-asserted LX6 reset
0xEE	LX6 firmware is running and ready
0xEF	Loading of S3 image done successfully
0xF0	Bootloader successfully verify signed image using 4K/2K key
0xF1	Bootloader identified as running on SP32P or multi-socket boot
0xF2	Security Policy check successful (only in secure boot)
0xF3	Bootloader successfully loaded SS3
0xF4	Bootloader successfully load fTPM Driver
0xF5	Bootloader successfully loaded sys_drv
0xF6	Bootloader successfully loaded secure OS
0xF7	Bootloader about to transfer control to secureOS
0xFC	Fatal error reported by another socket
0xFD	MP0 Data abort exception happened - PSP in debug unlockable state
0xFE	Uncorrectable error happened - PSP in debug unlockable state
0xFF	Bootloader sequence finished
BL_SUCCESS_BOOT_DONE	This is the Max Value for PostCode
0x7FFFFFFF	[UNUSED] Added to force this enum to 32-bits

Chapter 5. BMC Configuration Settings

5.1 Login

NOTE
For further details about the BMC, please refer to Norma BMC Manual for reference.
AIC® website link: https://www.aicipc.com

5.1.1 Required Browser Settings

Use a computer and configure its web browsers.

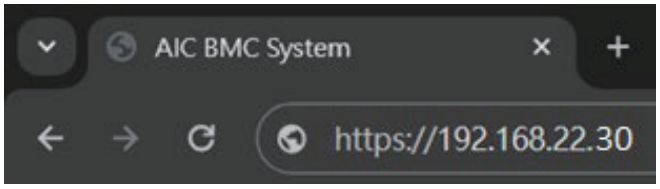
- Accept the file download when prompted in all browsers
- Javascript and cookie settings should be enabled in order to access the web site

NOTE
Cookies must be enabled in order to access the website.

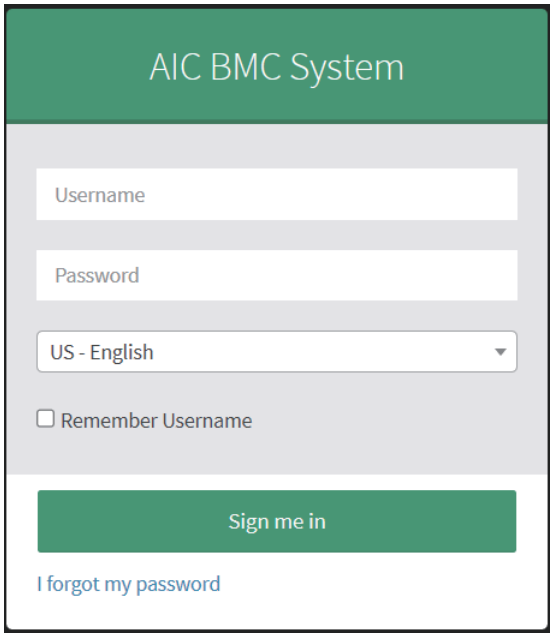
5.1.2 Username and Password

The computer and BMC need to be on the same subnet. After setting the static IP, they should be able to communicate. To establish a connection, follow the steps below.

1. Use the computer's terminal to ping the BMC IP address and ensure that it can be pinged.
2. If the BMC IP address is pingable, open a web browser on your computer, enter the BMC IP address in the URL bar.



3. Initial access prompts you to enter the User Name and Password. A sample screenshot of the login screen is given below.



Default Username: admin
Default Password: admin

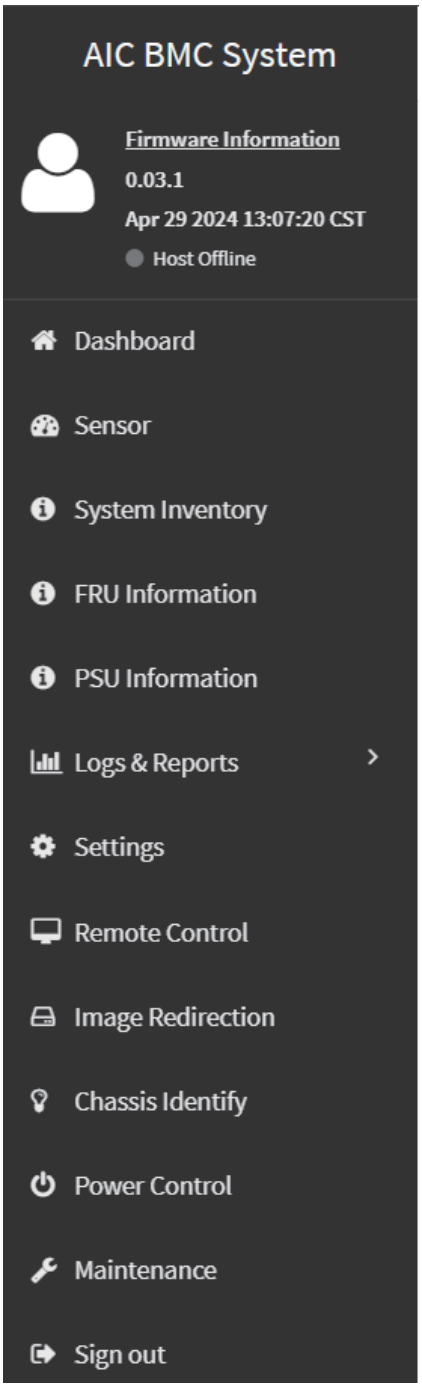
5.2 Web UI Common Features

For further details about the BMC, please refer to Norma BMC Manual for reference.
AIC® website link: https://www.aicipc.com

5.3 Menu Bar

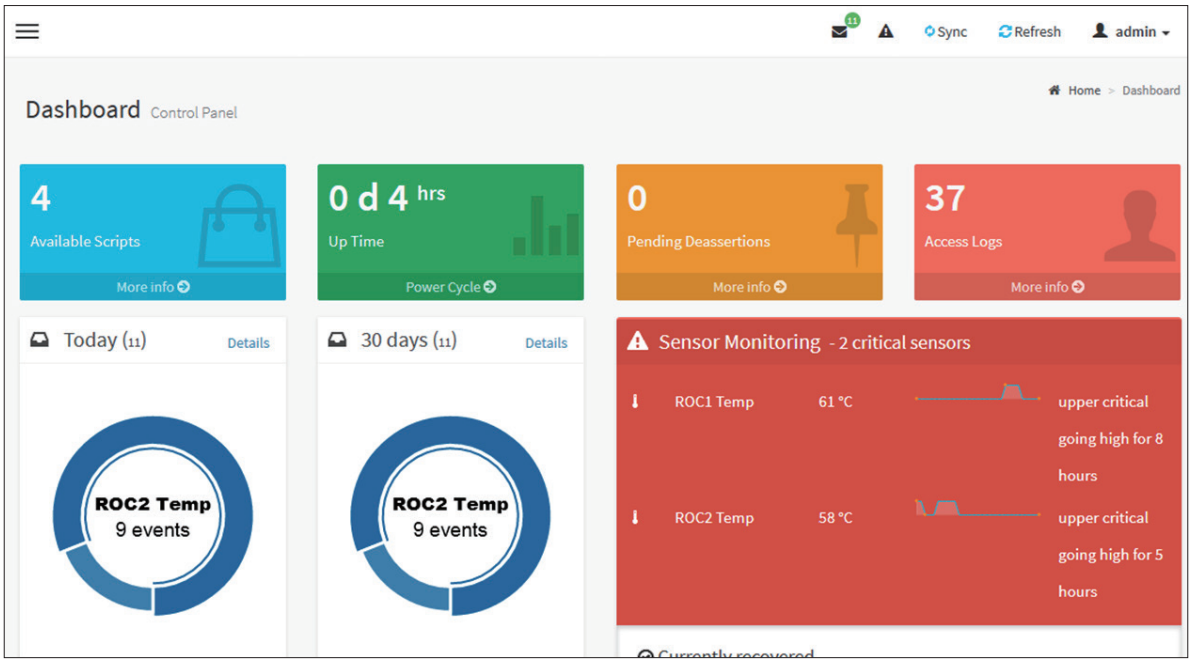
The menu bar displays the following.
Firmware Information will be displayed with the latest version, date and time details.
Power Control Status will be displayed as Host Online. To change the Power Control Status, click Host Offline link.

- Dashboard
- Sensor
- System Inventory
- FRU Information
- PSU Information
- Logs & Report
- Settings
- Remote Control
- Image Redirection
- Chassis Identify
- Power Control
- Maintenance
- Sign out



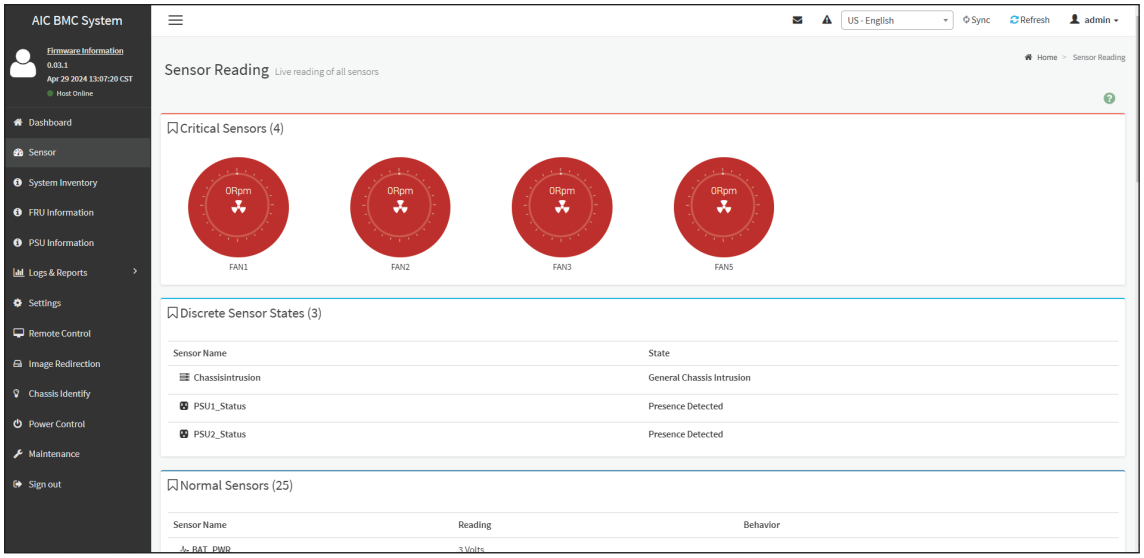
5.4 Dashboard

The Dashboard page gives the overall information about the status of a device.
To open the Dashboard page, click Dashboard from the menu bar. A sample screenshot of the Dashboard page is shown below.



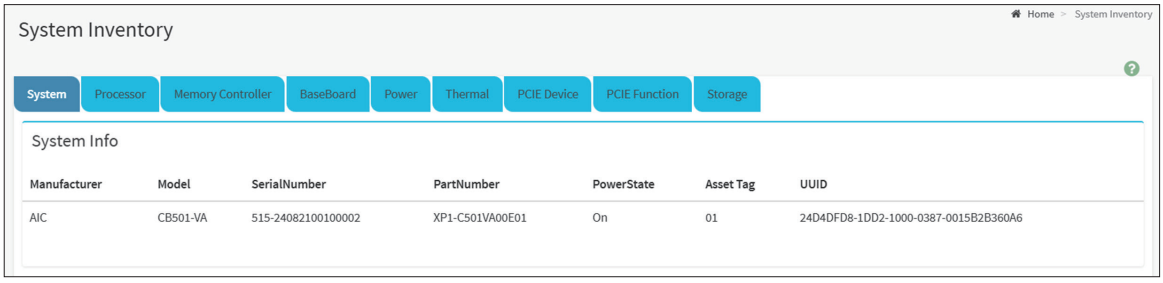
5.5 Sensor

The Sensor Reading page displays all the sensor related information.
To open the Sensor Reading page, click Sensor from the menu. Click on any sensor to show more information about that particular sensor, including thresholds and a graphical representation of all associated events.
A screenshot of Sensor Reading page is given below.



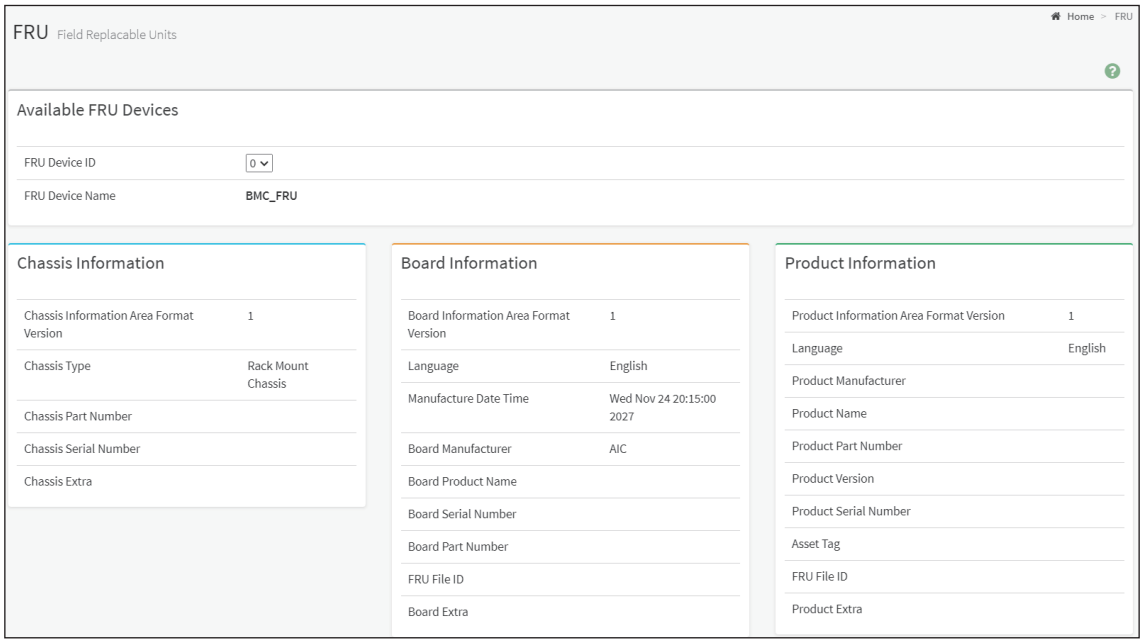
5.6 System Inventory

To open System Inventory main page, click System Inventory from the menu bar.
A screenshot displaying the menu items under System Inventory is shown below:



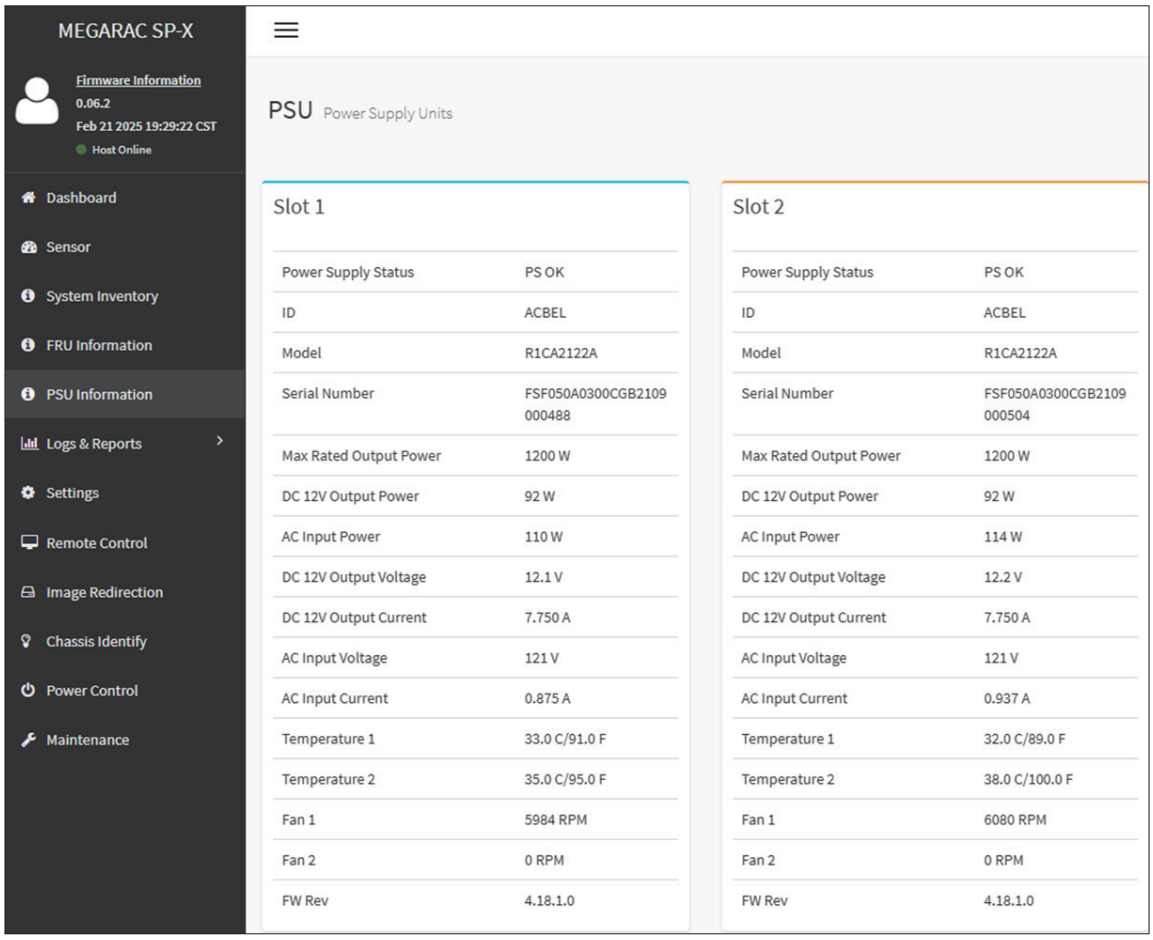
5.7 FRU Information

FRU Information page displays the BMC's FRU device information. FRU page shows information like Basic Information, Chassis Information, Board Information and Product Information of the FRU device.
To open the FRU Information page, click FRU Information from the menu bar. Select a FRU Device ID from the FRU Information section to view the details of the selected device. A screenshot of FRU Information page is given below.



5.8 PSU Information

To open the PSU Information page, click PSU Information from the menu bar. A screenshot of PSU Information page is given below.

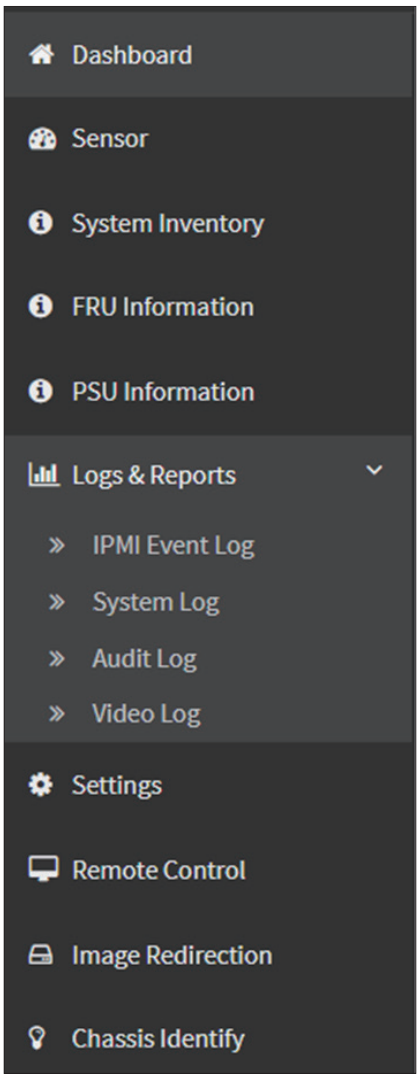


5.9 Logs & Reports

To open the Logs & Reports page, click Logs & Reports from the menu bar. The Logs & Reports page displays the following information.

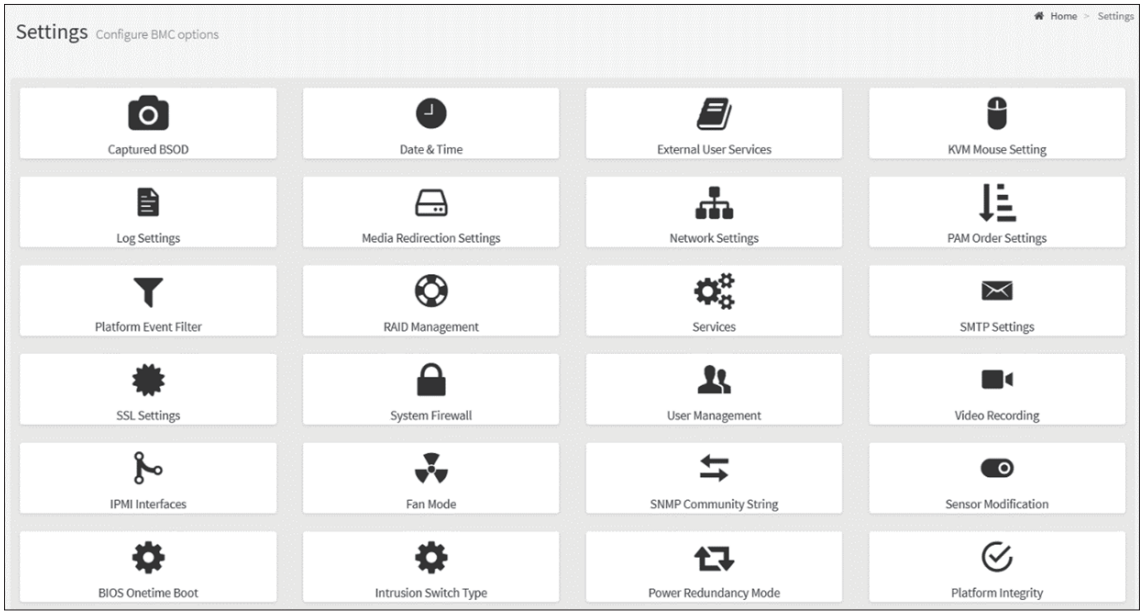
- IPMI Event Log
- System Log
- Audit Log
- Video Log

A screenshot displaying the menu items under Logs & Reports is shown below



5.10 Settings

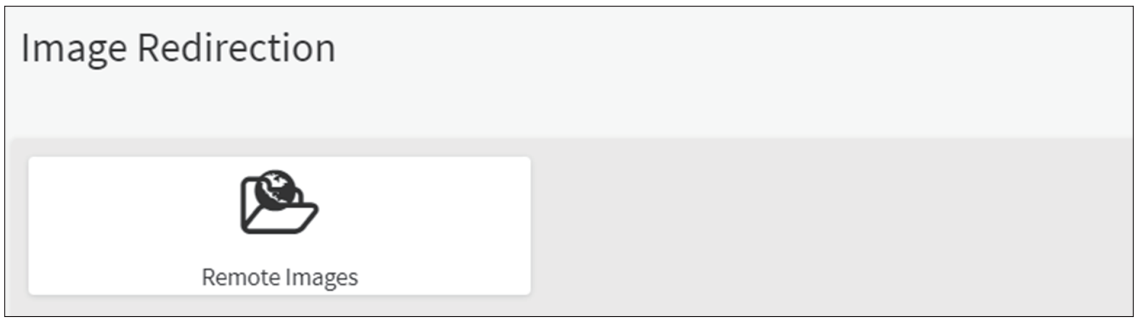
To open the Settings page, click Settings from the menu bar. This group of pages allows you to access various configuration settings. A screenshot of Configuration Group menu is shown below.



A detailed description of the Configuration menu is given below.

5.11 Images Redirection

This page is used to configure the images into BMC for redirection. This can be done either by uploading an image into BMC say, **Local Media** or by mounting the image from the remote system, **Remote Media**.
To open Images Redirection page, click Images Redirection from the menu bar.
A sample screenshot of Images Redirection page is shown below.



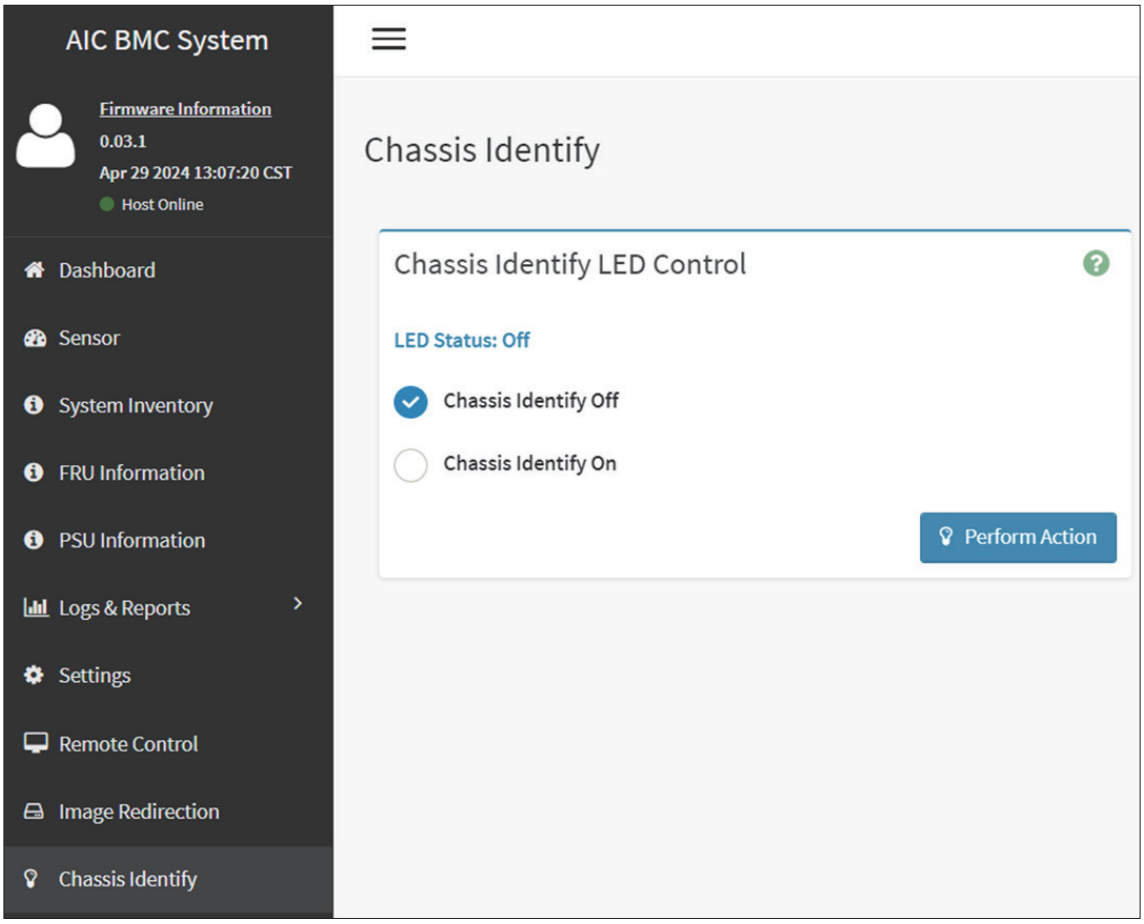
The fields of Images Redirection page are explained below.

- Remote Images

NOTE
Media will always be redirected using the lowest available instance number, regardless of the instance slot opted in Web UI. This is applicable for both local and remote media images.

5.12 Chassis Identify

To open Chassis Identify, click Chassis Identify from the menu bar. A sample screenshot of Chassis Identify is shown below.

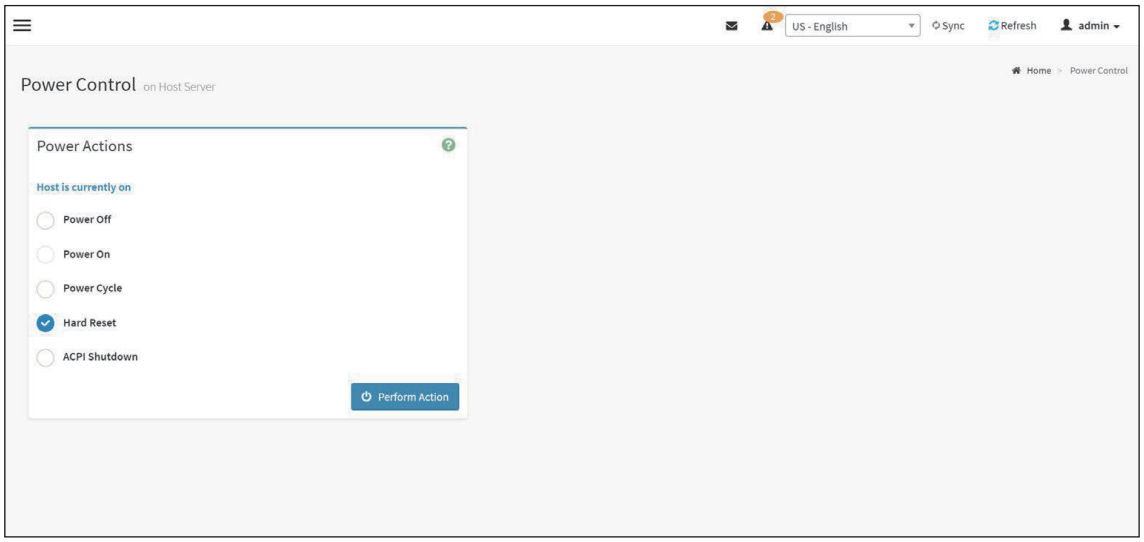


The various options of Chassis Identify are given below.

- Chassis Identify Off: This option will turn off the Chassis Identify LED.
- Chassis Identify On: This option will turn on the Chassis Identify LED.

5.13 Power Control

This page allows you to view and control the power of your server.
To open Power Control, click Power Control from the menu bar. A sample screenshot of Power Control is shown below.

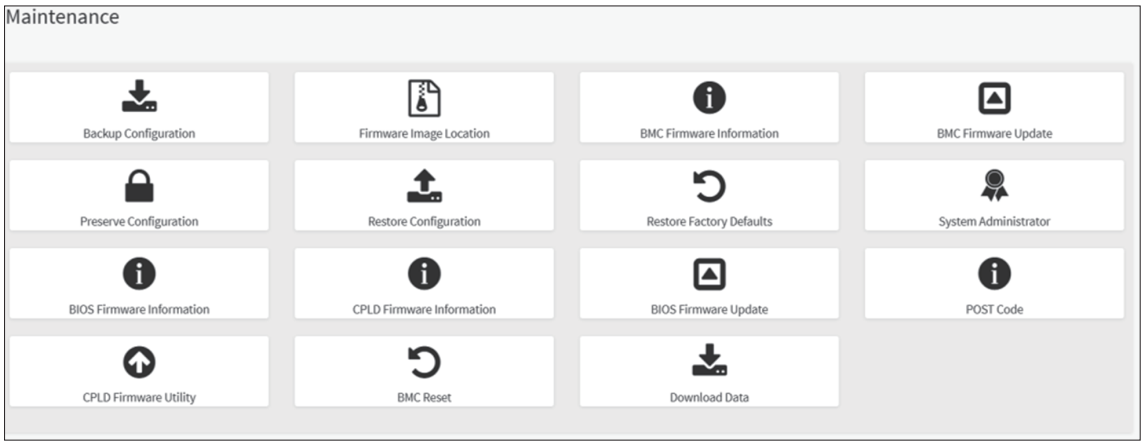


5.14 Maintenance

To open the Maintenance page, click Maintenance from the menu bar. This group of pages allows you to do maintenance tasks on the device. The menu contains the following items:

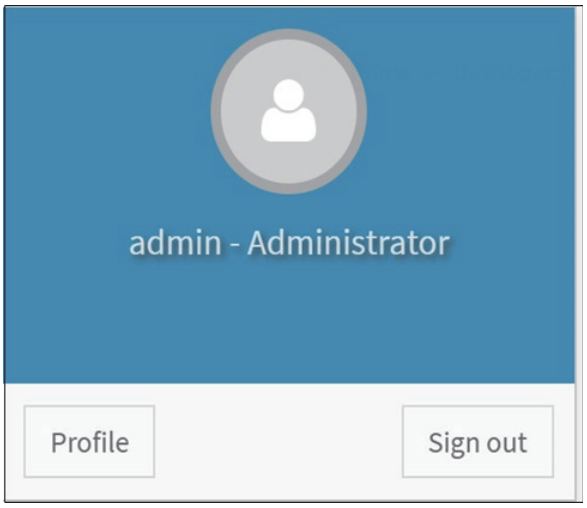
- Backup Confifiguration
- Firmware Image Location
- BMC Firmware Information
- BMC Firmware Update
- Preserve Confifiguration
- Restore Confifiguration
- Restore Factory Defaults
- System Administrator
- BIOS Firmware Information
- CPLD Firmware Information
- BIOS Firmware Update
- CPLD Firmware Update
- POST Code
- BMC Reset
- Download Data

A sample screenshot of Maintenance page is displayed below.



5.15 Sign Out

To log out from, click the admin on the top right corner of the screen. A sample screenshot of admin option is shown below.



Click **Sign Out** to perform log out. A Warning message will be prompted you to proceed further, click **OK** to log out or **Cancel** to retain the interface.

Chapter 6. Technical Support

www.aicipc.com

Global Headquarters
Address: No. 152, Section 4,
Linghang N. Rd, Dayuan District,
Taoyuan City, Taiwan 337
Tel: +886-3-433-9188
Fax: +886-3-287-1818
Sales Email: sales@aicipc.com.tw
Support Email: support@aicipc.com

China Office
Address: Room 215, Building 4, No. 471
Guiping Road, Xuhui District,
Shanghai City, 200233 China
Tel: +86-21-5496-1421
Sales Email: sales@aicipc.com.cn
Support Email: support@aicipc.com

Korea Office
Address: KB616, 217, Hyangdong-ro,
Deogyang-gu, Goyang-si,
Gyeonggi-do, Republic of Korea
Sales Email: sales@aicipc.co.kr
Support Email: support@aicipc.co.kr

USA Headquarters (SoCal)
Address: 21808 Garcia Lane
City of Industry, CA 91789,
United States
Toll free: + 1-866-800-0056
Tel: +1-909-895-8989
Sales Email: sales@aicipc.com
Support Email: support@aicipc.com

USA Office (NorCal)
Address: 48531 Warm Springs Boulevard
Suite 404
Fremont, CA 94539, United States
Tel: +1-510-573-6730
Sales Email: sales@aicipc.com
Support Email: support@aicipc.com

USA Office (New Jersey)
Address: 322 Route 46 West
Suite 100
Parsippany, NJ 07054
United States
Tel: +1-973-884-8886
Sales Email: sales@aicipc.com
Support Email: support@aicipc.com

The Netherlands Office
Address: Peppelkade 58, 3992AK, Houten,
The Netherlands
Tel: +31-30-638-6789
Fax: +31-30-636-0638
Sales Email: sales@aicipc.nl
Support Email: support.nl@aicipc.nl

For additional technical support or questions about trouble shooting, please contact the AIC® representative nearest to you or visit our AIC® website for more information.
AIC® website: https://www.aicipc.com/faqs/.